WIZ-IP51S User Manual

V1.0

☞ For more information, visit our website at http://www.wiznet.io

Document Revision History

Version	Date	Note
V1.0	2025/08/07	First release

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1 Introduction

1.1 Overview

The WIZ-IP51S is a network offloading module that integrates the W5100S chip (with built-in PHY physical layer and TCP/IP hardware protocol stack) and an RJ45 connector with integrated network transformer. As a plug-and-play component, it enables seamless interface connection between the W5100S and the transformer without the need for additional circuit design.

For users who wish to quickly develop networked systems, the WIZ-IP51S is an ideal choice.

Note: For detailed information regarding the hardware TCP/IP protocol stack, please refer to W5100S datasheet.

- Network port connector section: Integrated network transformer network port (including W5100S chip, network transformer and RJ45).
- TCP/IP protocol stack and Ethernet MAC: Implemented by W5100S chip.
- Ethernet PHY: Integrated by W5100S chip.

1.1.1 Functional Features

- Supports full hardware TCP/IP protocol: TCP, UDP, WOL, ICMP, IGMPv1/v2, IPv4, ARP, PPPoE
- Supports SOCKET-less instructions: ARP-request, PING-request
- Supports 4 independent SOCKET concurrent communication
- Supports half-duplex/full-duplex operation mode
- Supports Ethernet power-off mode and master clock selection energy-saving mode
- Supports UDP-based network wake-up (WOL) function
- High-speed SPI interface (MODE 0/3)
- Built-in total 16Kbytes of send/receive cache
- Integrated 10BaseT/100BaseTX Ethernet PHY
- Supports Ethernet auto-negotiation (full/half-duplex, 10Base-T/100Base-TX)
- Supports Auto-MDIX function (only supported in Ethernet auto-negotiation mode)
- Operating voltage: 3.3V (I/O compatible with 5V signal voltage)
- 19-pin pin header interface
- Package size (length×width×height):32.5×16.5×17.3(mm)
- Compatible with WIZnet's IO module carrier board development board

1.1.2 Product Features

- All-hardware TCP/IP protocol stack network chip W5100S
- Ethernet
  - 10/100Mbps Adaptive Ethernet
- Connect to the host interface
  - Standard SPI：MISO、MOSI、CLK、CSn
- Power supply
  - Input power supply：3.3V DC
- Mechanical parameters
  - Dimensions (length ×width×height):32.5×16.5×17.3(mm)
- Operating temperature
  - Industrial grade: -40~+85℃
- Storage temperature
  - -40~+85℃,5~95%RH

1.2 Product Specifications

1.2.1 Electrical Parameters

1.2.1.1 Power Parameters

Unless otherwise specified, the parameters listed in Table 1-1 and Table 1-2 refer to the values at a temperature of 25℃.

Table 1-1 Power supply parameters

Numbering	Category	Specification			
		Minimum	Typical	The greatest	Organization
VDD	Module voltage	2.97	3.3	3.63	V
I	Module current	124	130	137	mA

1.2.1.2 Power Consumption Parameters

Table 1-1 Power consumption parameters

Working condition	Test value (mA)	Working condition	Test value (mA)
Standby	43	100Mbps Connectionless	42
10Mbps Connectionless	25	100 Mbps for data communication	130
100 Mbps for data communication	130		

1.2.2 Mechanical Dimensions

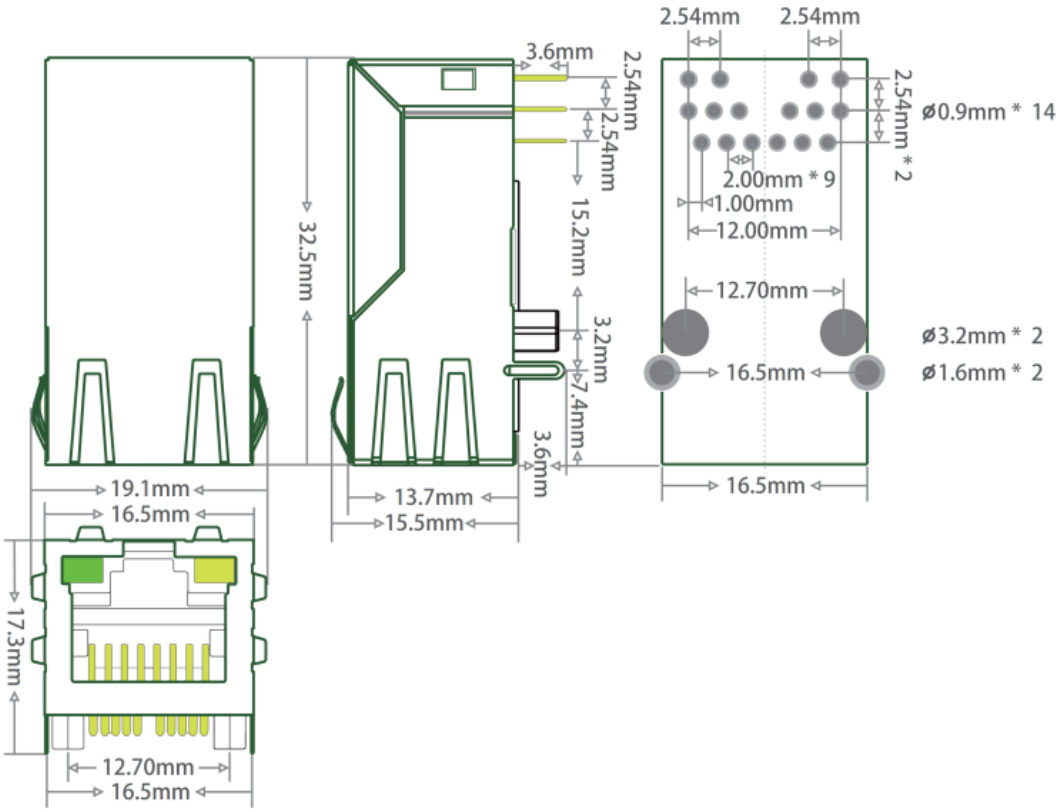

Figure 1-1 All views of the product

1.2.3 Temperature Characteristics

Table 1-2 Temperature Characteristics

Name	Level	Operating temperature	Storage temperature
WIZ-IP51S	Industrial grade	-40~+85℃	-40~+85℃

2 Hardware Section Description

2.1 Pin Layout Description

Now, we will introduce the pins of WIZ-IP51S and the usage of the IO module carrier board of the accompanying evaluation board respectively.

The appearance of WIZ-IP51S is shown in Figure 2-1.

Figure 2-2 is the pin layout diagram of WIZ-IP51S, and Table 2-1 provides the pin description for WIZ-IP51S.

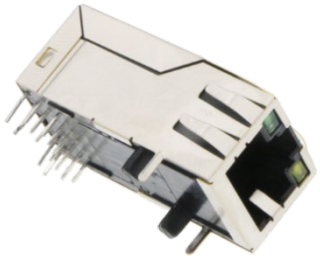

Figure 2-1 The external appearance diagram of the WIZ-IP51S module

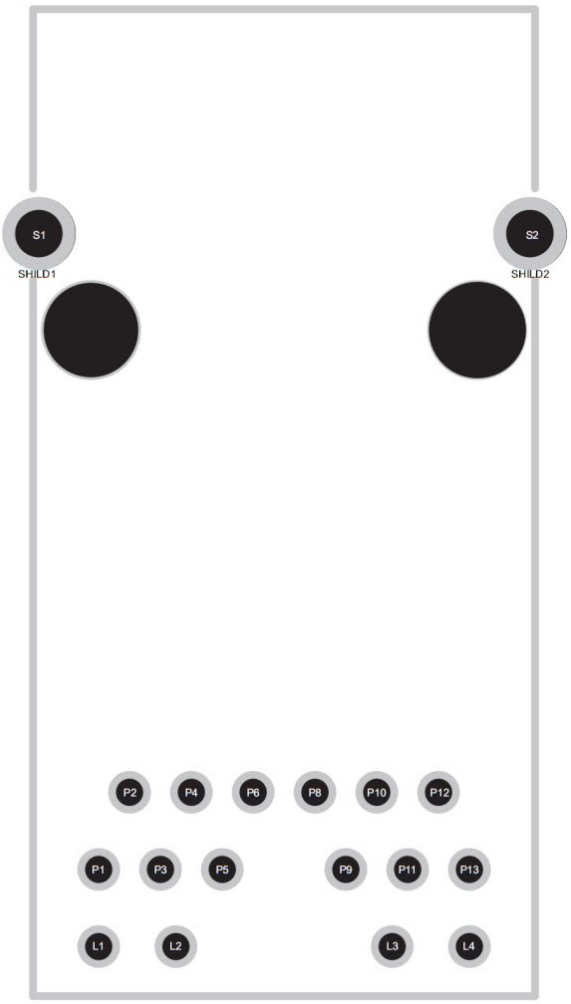

Figure 2-2 WIZ-IP51S Pin Assignment

Table 2-1 Pin Description

Pin number	Pin name	Function
P1	ACT_LED	Data reception/transmission activity indicator light
P2	VCC	3.3V Power pin
P3	GND	Power ground
P4	CSn	SPI interface chip selects signal pin, with low level as the effective state
P5	CLK	SPI clock input pin
P6	MISO	SPI master input, slave output
P8	MOSI	SPI master output from slave input
P9	INTn	Interrupt output pin, low level is effective
P10	RESETn	Reset pin, low level effective (must be maintained for at least 500us)
P11	NC	Retention function
P12	NC	Retention function
P13	LINK_LED	Network connection indicator light
L1	LED1-	Connect to P1
L2	LED1+	Connected in series with the resistor to VCC
L3	LED2+	Connected in series with the resistor to VCC
L4	LED2-	Connect to P13
S1	SHILD1	Shell
S2	SHILD2	Shell

2.2 Introduction to the Evaluation Board

The IO module carrier board is an evaluation board that facilitates users to test and apply the modules. This evaluation board integrates the mainstream single-chip microcontroller STM32F103RCT6 and the USB to TTL converter chip CP2102.The schematic diagram of the IO module carrier board is shown in Figure 2-3.

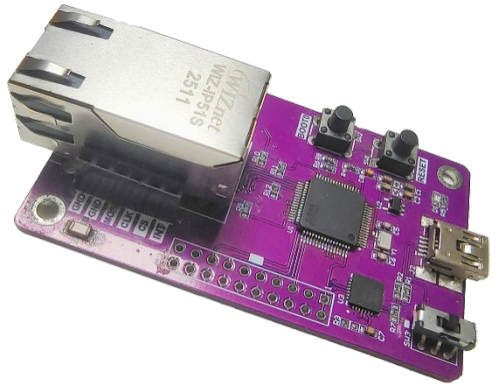

Figure 2-3 IO module carrier board outline drawing

- The USB Mini interface provides the evaluation board with 5V DC power supply and one serial port for the MCU, which can be used for ISP-style program download and data communication testing.
- Key Instructions for IO Module Carrier Board

Table 2-2 IO module carrier board Key Instructions

Numbering	Explanation
RESET（SW1）	Hardware reset button
BOOT（SW2）	Enter the BOOT button of the microcontroller

- Program download method for IO module carrier board

The IO module carrier board supports the ISP download method. The operation steps are as follows: first, press and hold the BOOT button, then press the RESET button once, and finally release the BOOT button. This will enable you to enter the program download mode. Open the ISP tool of STM32 and select the corresponding firmware to complete the download.

- The reference design schematic diagram of the peripheral circuits for WIZ-IP51S is shown in Figure 2-4.

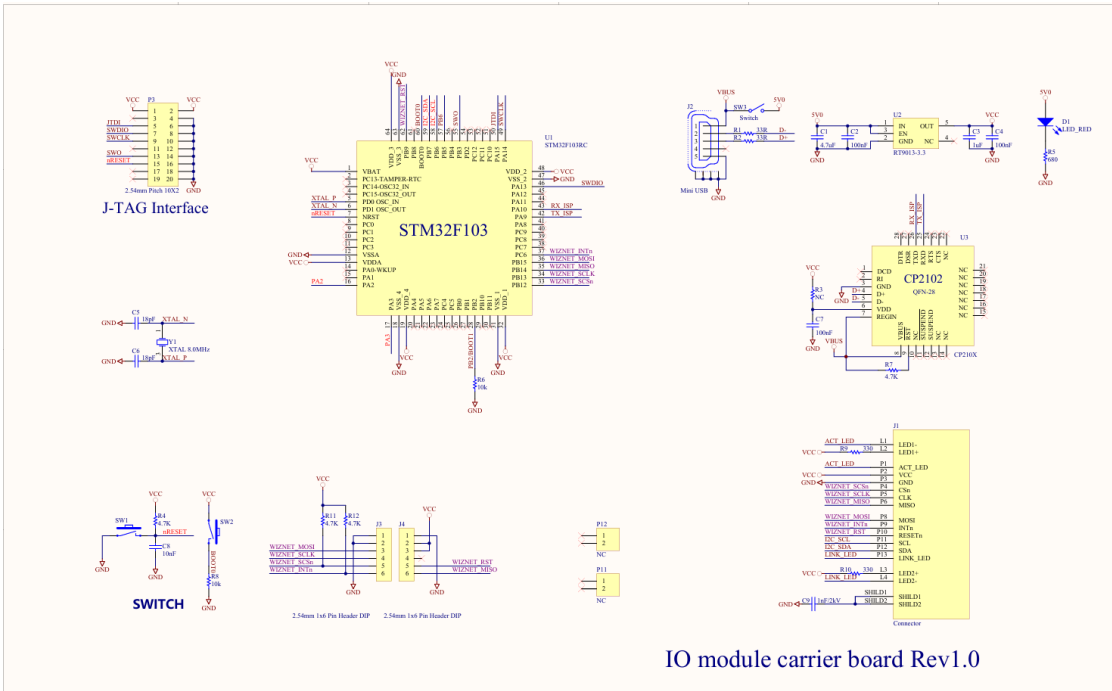

Figure 2-4 Reference design schematic diagram of the peripheral circuit of WIZ-IP51S

2.3 Quick Evaluation Board Wiring Instructions

Users can download the corresponding reference code for W5100S from www.w5500.com and burn it onto the IO module carrier board for performance testing and evaluation, as shown in Figure 2-5.

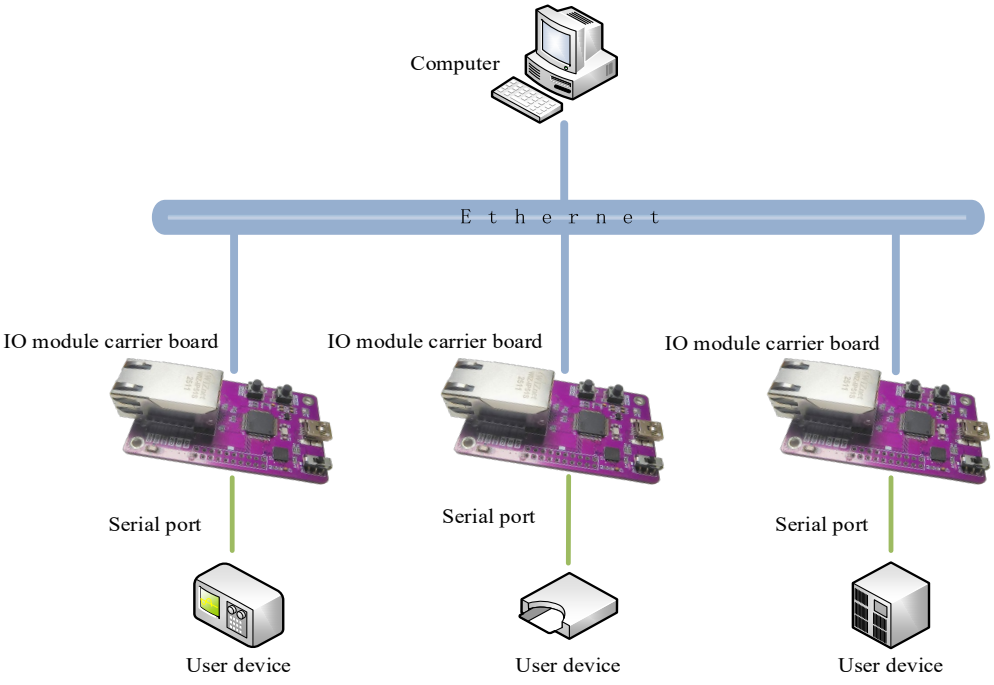

Figure 2-5 Test and Evaluation Schematic Diagram of IO Module Carrier Board

3 SPI operations

The SPI configuration method of WIZ-IP51S is detailed in the following W5100S datasheet.

4 Timing Diagram

4.1 Reset Timing

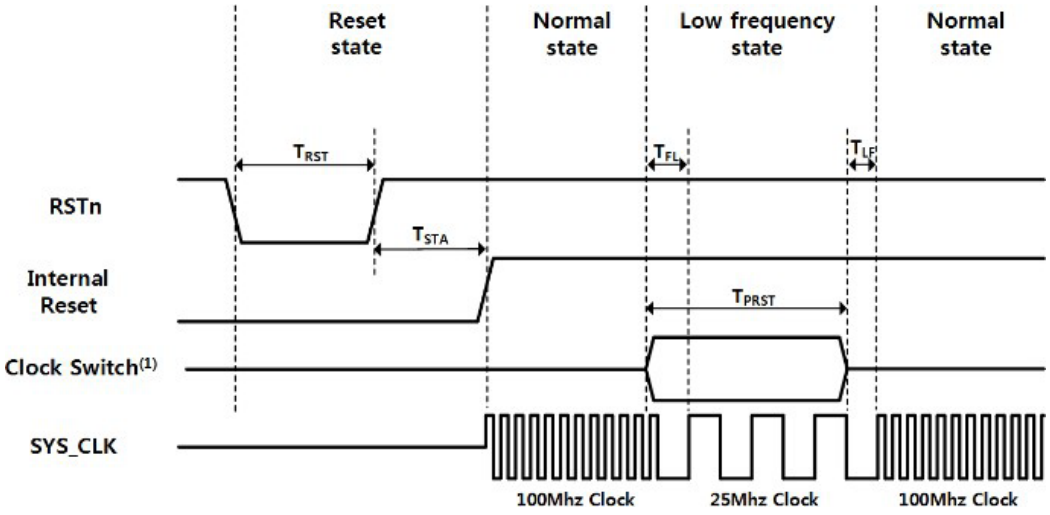

Figure 4-1 Reset Timing

Table 4-1 Reset Timing Table

Flag bit	Description	Min	Typical	Max
T_{RST}	Reset time	210ns	330ns	560ns
T_{STA}	Stable time	-	-	60.3ms

4.2 SPI Access Read Timing

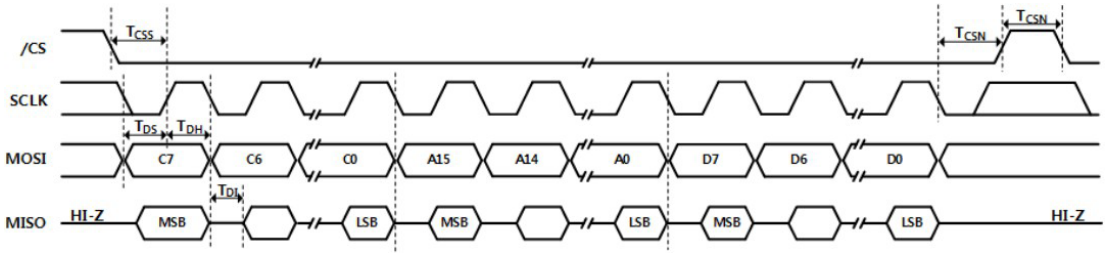

Figure 4-2 SPI Read Timing

Table 4-1 SPI Read Timing

Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency	-	70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK	-	ns
T_{CSN}	SCSn Next Time	2 SYS CLK	-	ns
T_{DS}	Data In Setup Time	3	-	ns
T_{DH}	Data in Hold Time	3	-	ns
T_{DI}	Data Invalid Time	7	-	ns
T_{DR}	Data Ready Time	6 SYS CLK+30	-	ns

4.3 SPI Access Write Timing

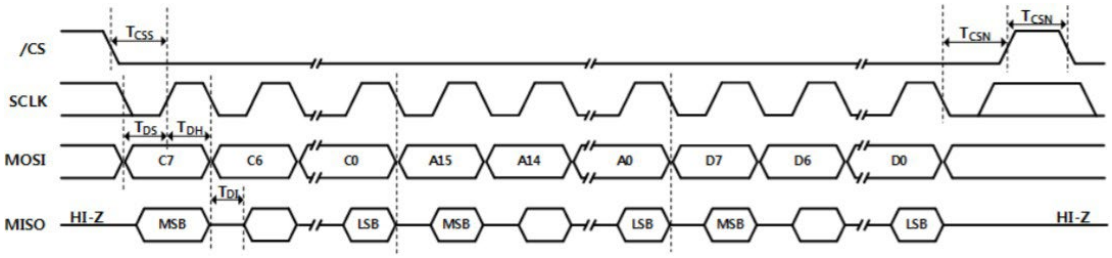

Figure 4-3 SPI Write Timing

Table 4-3 SPI Write Timing

Flag bit	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency	-	70	MHz
T_{CSS}	SCSn Setup Time	3 SYS_CLK	-	ns
T_{CSN}	SCSn Next Time	3 SYS_CLK	-	ns
T_{DS}	Data In Setup Time	3	-	ns
T_{DH}	Data In Hold Time	3	-	ns
T_{DI}	Data Invalid Time	7	-	ns