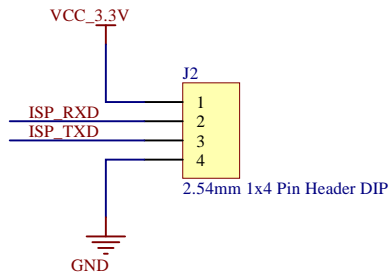
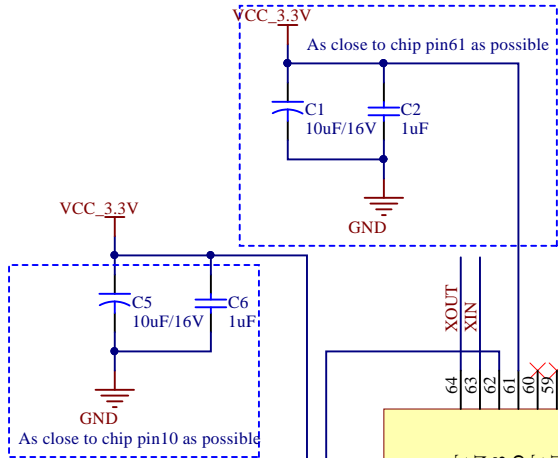
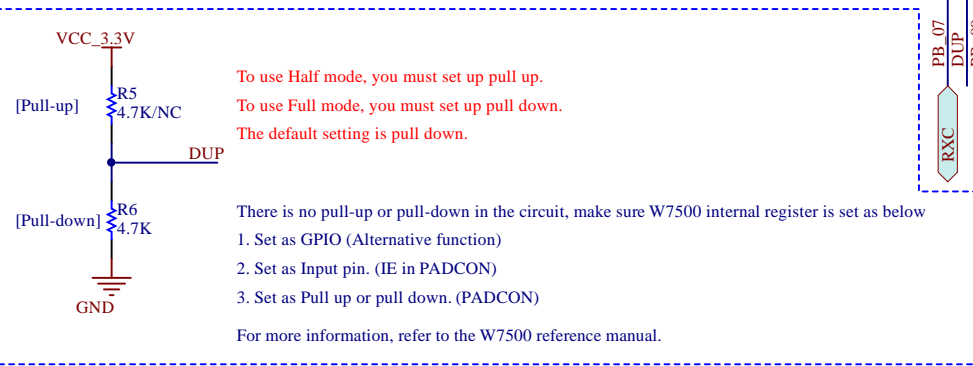


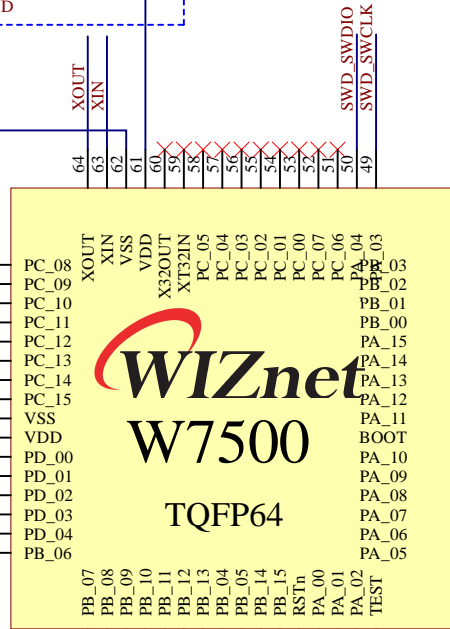
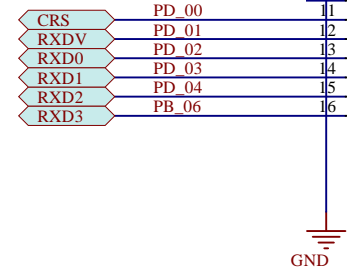
MAIN CLOCK



ISP UART2

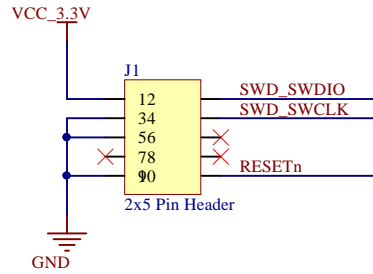


As close to chip pin10 as possible

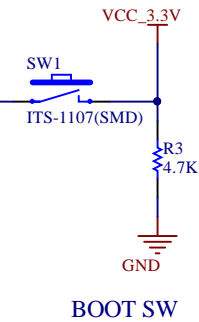


MDIO(PB\_14),MDC(PB\_15) pin is should be handled as GPIOs.

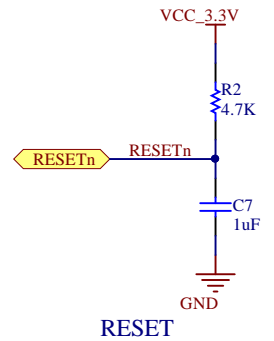
PA\_00 is PHY LINK check pin(input). This pin checks PHY link from peer  
 This pin should be connected to the LINK status signal of the RJ-45.



U1 W7500

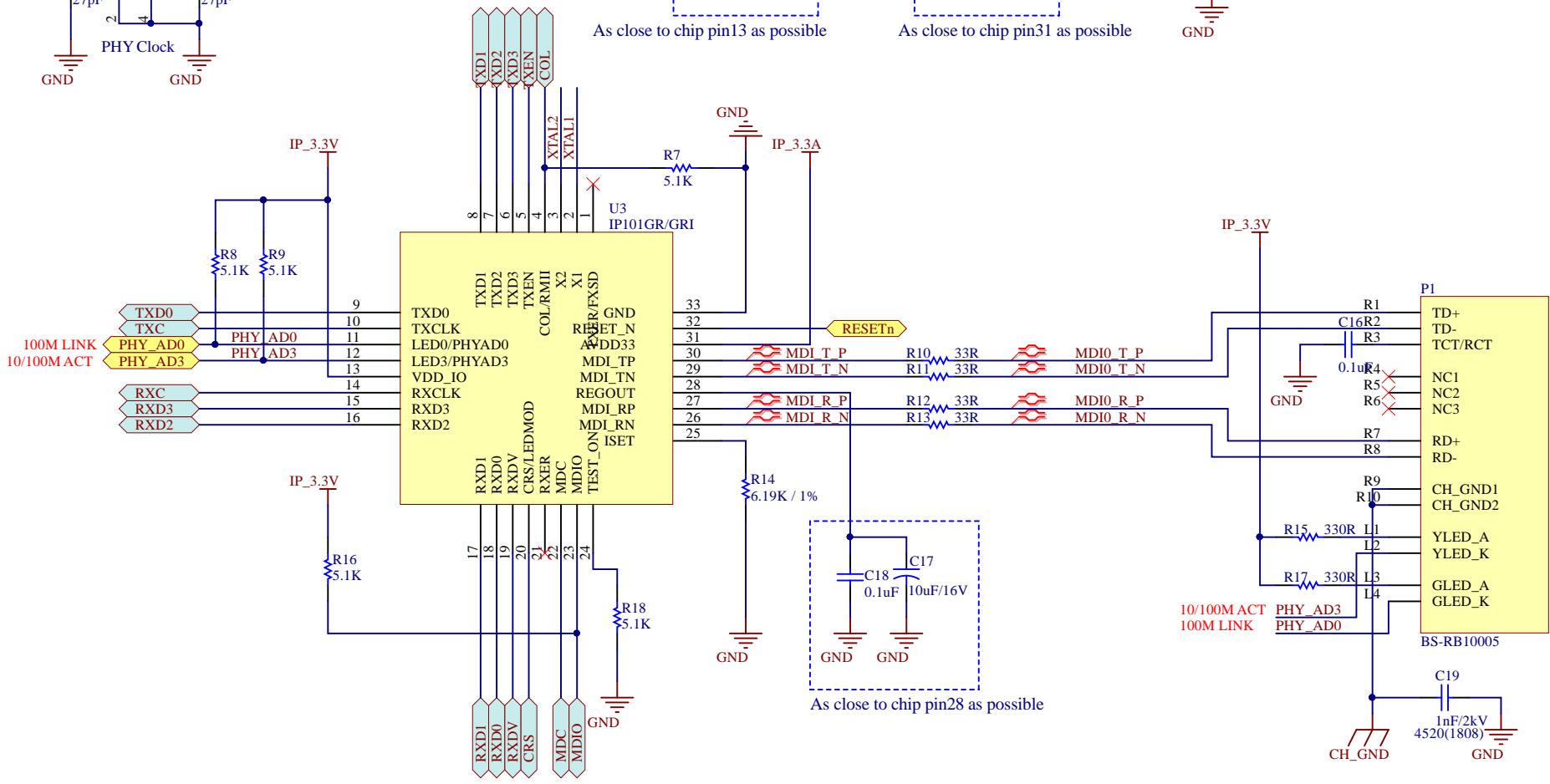
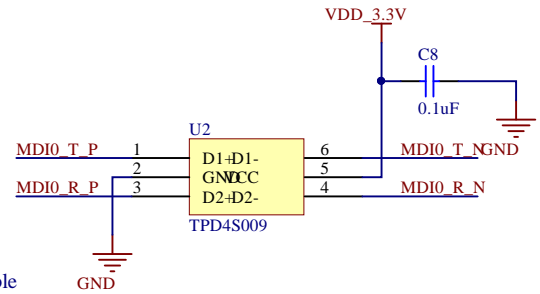
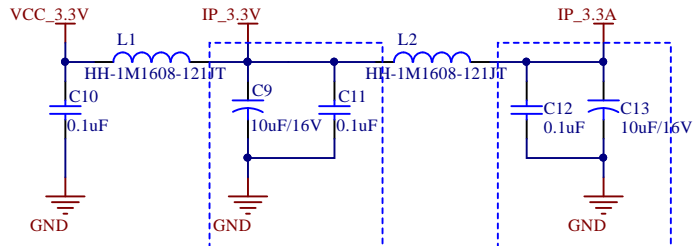
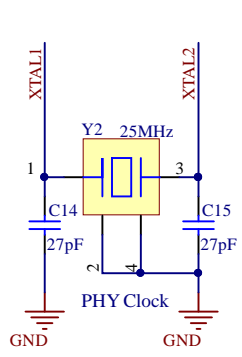


BOOT SW



RESET

Title			WIZnet Co., Ltd. 5F, Humax Village Hwangseoul-ro, Bundang-gu Seongnam-si, Gyeonggi-do South Korea	
Size: A4	Number:	Revision:		
Date: 2017-05-25	Sheet 1 of *			
Team: Team Wiki	Drawn By: Edward			



Title			5F, Humax Village Hwangseaul-ro, Bundang-gu Seongnam-si, Gyeonggi-do South Korea	
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Date: 2017-05-25	Sheet2 of *			
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