QRT semiconductor

Reliability Test Report

QRT semiconductor assists you in developing and assessing custom products. Because of Accredited Laboratory of Korea Laboratory Accreditation Scheme, reliability test procedures are recognized internationally (KOLAS certification by Mutual Recognition Arrangement).

Company: WIZnet Co., Ltd.
Product: W5200
Package Type: 48 QFN
Purpose: Reliability Test
Date: 16 Dec, 2011
Document No: IRRP-1110-00218

Prepared by :*Hyunbae Lee*

Approved by :*Jinsu Lee*

: *Changjoon Lee*

QRT SEMICONDUCTOR

1 Qualification Plan and Results

The purpose of these tests is evaluation (or monitoring) of W5200. Test conditions are specified in customers in-house test plan and all test procedures comply with JEDEC standards.
Obligation to perform exact procedure to reference documents is QRT semiconductor responsibility only, but establishing failure criteria and judgment of pass/fail is customer's responsibility.

TEST MODE	TEST CONDITION	TEST TIME	SAMPLE SIZE	FAILED UNIT [1]	REF. DOCUMENT [2]
High temperature Operating Life	125 ℃ , VDD33 (V0) : 3.3 V VDD (V4) : 1.8 V, VIH : 3.3 V, VIL : 0 V	504 h	77	0	JESD22-A108C
Low temperature Operating Life	-40 ℃ , VDD33 (V0) : 3.3 V VDD (V4) : 1.8 V, VIH : 3.3 V, VIL : 0 V	504 h	77	0	JESD22-A108C

NOTE:
[1] Test results are based on the "Notice of Final Test Result" provided by WIZNET.
[2] Although the name of test item is same, reference documents can be JEDEC, MIL-std or AEC.

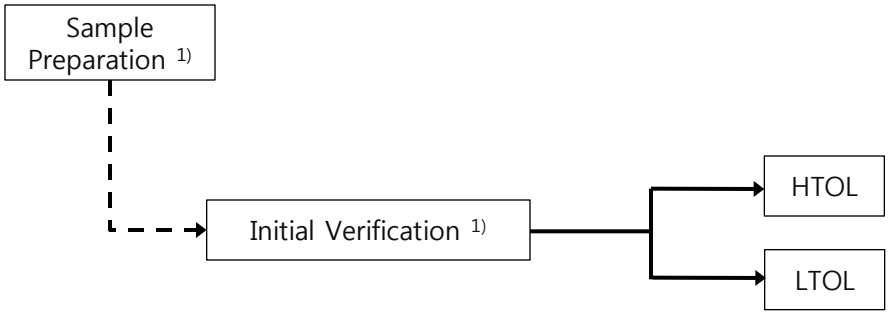
2 Test Vehicles

Information

Manufacturer :	WIZNET
Part Number :	W5200
Description :	-
Package Type :	48 QFN
Ass'y Site :	-
Fab Site :	-

3 Test Flow/Procedure

All reliability Tests performed by QRT semiconductor was ensured with KOLAS accreditation. Entire test schematics is the same as below.



NOTE 1) Customer's Responsibilities only.

Figure 1. Reliability Test Flow

4 Reliability Tests

4.1 High Temperature Operating Life Test (HTOL)

The High Temperature Operating Life (HTOL) or steady-state life test is performed to determine the reliability of devices under operation at high temperature conditions over an extended period of time. It consists of subjecting the parts to a specified bias or electrical stressing, for a specified amount of time, and at a specified high temperature .

Conditions			
User Temp (T_u)	55 ℃	Test Temp (T_t)	125 ℃
User Voltage (V_u)	-	Test Voltage (V_t)	Vcc : max
Activation Energy (E_{aa})	0.7	$\gamma V = (K/X)$	-
Sample size (N)	77	failures (f)	0
Test duration (t_A)	504	t_{life} (for ppm)	12 months

Life estimate is calculated on the assumption that 1) Gate short to source or drain *, 2) User temp is 55 ℃.
*Failure Mode: Gate short to source or drain
*Failure Mechanism: Intrinsic breakdown; for gate oxide thickness >4 nm
* E_{aa} = 0.7 (activation energy reference “JEP122D”)

---------Calculation----------

Acceleration Factor (AF) $= \exp\{(E_{aa}/k)(1/T_{use} - 1/T_{test})\}$
where
Eaa = apparent activation energy in eV/atom
k = Boltzmann’s constant (8.62×10^{-5} eV/K)
T_{use} = use temperature in kelvins
T_{test} = Test temperature in kelvins

$= \exp[(0.7/k) \times (1/328 – 1/398)] = 77.94$
∴ Test time = AF × Test Time = 77.94 × 504 = 4.48 years

if Exponential distribution (FIT Calculation)
The degrees of freedom = 2, and $\chi^2 = 1.83$ @ CL 60%
Failure rate (in FIT) = $10^9 \times \chi^2_{c,d} / (2 \times AF \times N \times t_A)$
$= 10^9 \times 1.83 /(2 \times 77.94 \times 77 \times 504) = 303$ FIT

∴ Failure Rate (in ppm, 12 months) = 2 654 ppm during the first 12 months of usage.
∴ MTTF = 376.8 years

! Disclaimer !
This estimation is an example of JESD74A. Voltage Acceleration is excluded in this procedure.
Voltage acceleration and actual use temperature must be considered for a better output.
Calculation is for information only.

4.2 Low Temperature Operating Life (LTOL)

This test is intended to look for failures caused by hot carriers, and is typically applied on memory devices or devices with submicron device dimensions.

Test Condition

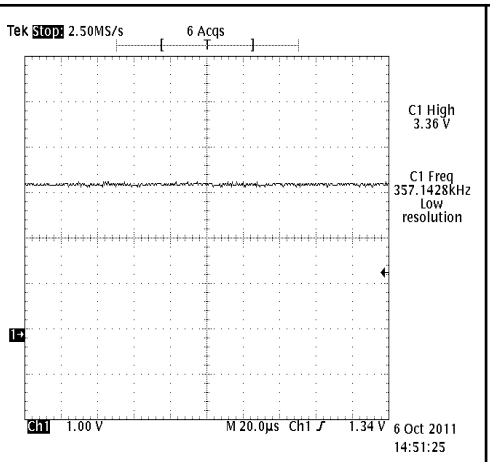
Temperature: - 40 (- 5, + 0) ℃
Bias Configuration: VDD33 (V0) : 3.3 V, VDD (V4) : 1.8 V, VIH : 3.3 V, VIL : 0 V
Duration: 504 hours
Sample Size: 77 ea

APPENDIX A: HTOL Test Conditions

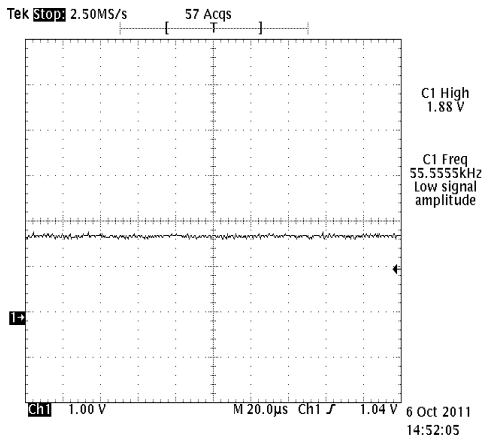
1. Bias Configuration

HTOL Board Density : 80 ea / Board	Load S/S : 77 ea / Board
VDD33 (V0) : 3.3 V VDD (V4) : 1.8V	VIH : 3.3 V VIL : 0 V
Vector Type : CHAIN_EWZ001.TSTL2	Cycle Time : 1000 ns
Timing Format Condition	
Remark : ◈. Signal Rate : 1000 ns ◈. Frequency : 1 Mhz ◈. ANE" { force { format RZ; start 500, stop 1000ns; } }	

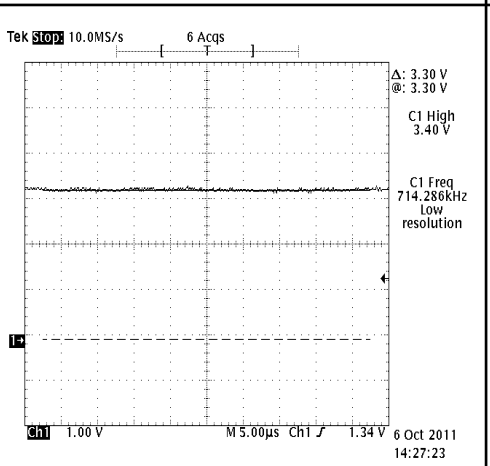
2. Output signal



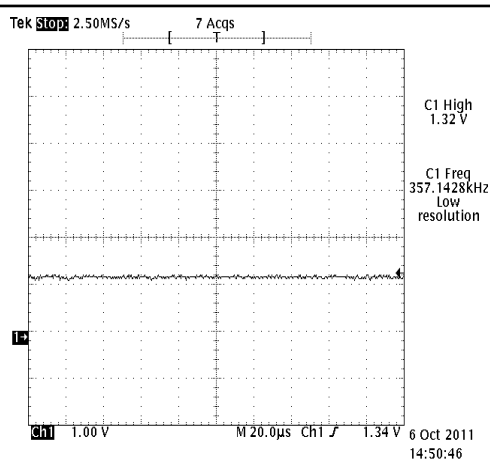
V0
3.3V



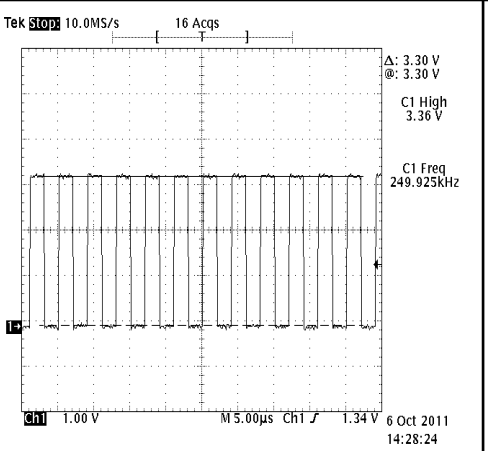
V4
1.8V



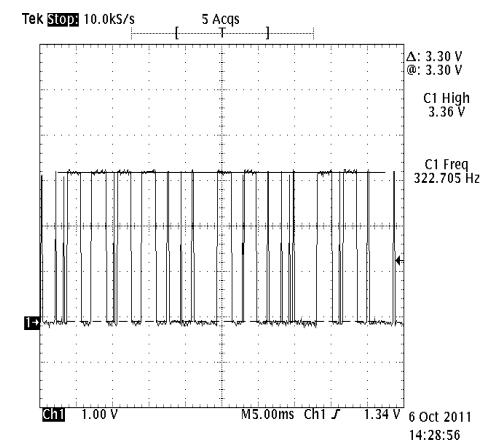
O_XO
Pin #2



V_BIAS
Pin #12

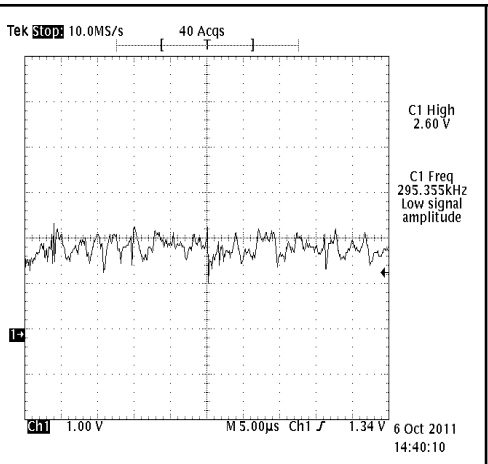


B_MDIO
Pin #7

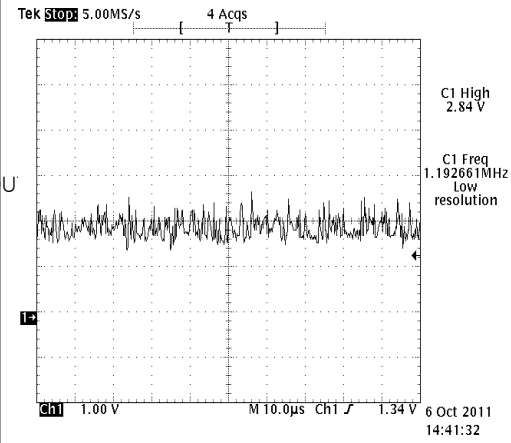


B_MDIO
Pin #7

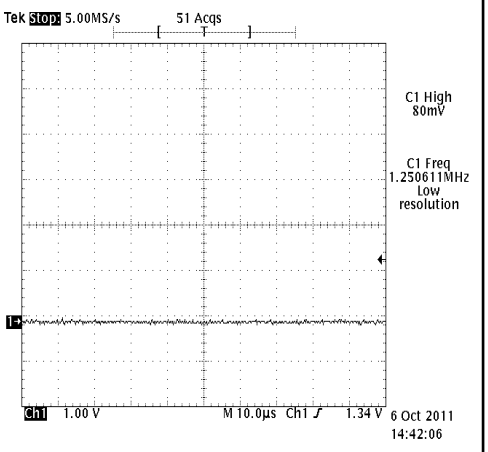
2. Output signal (cont'd)



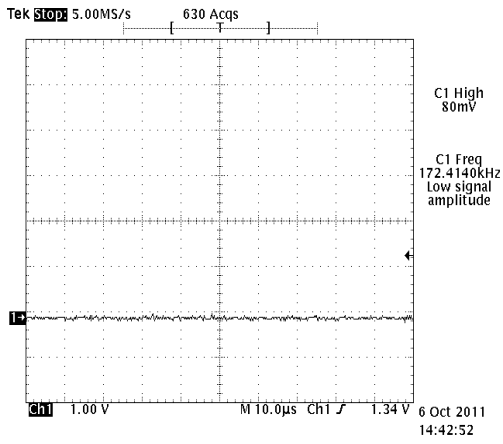
B_POWERCU
Pin #14



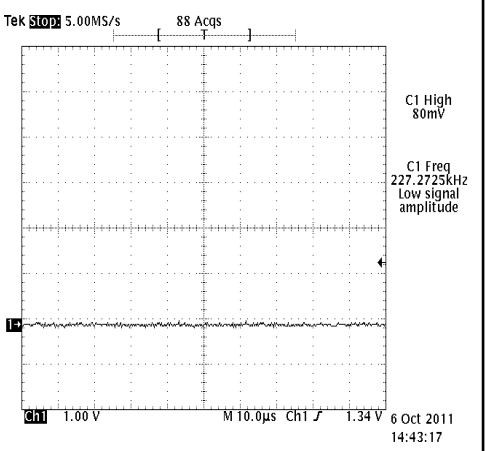
B_XTAL_VDD
Pin #16



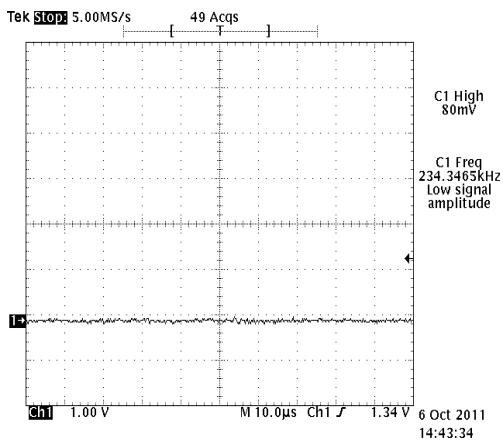
B_TXP
Pin #17



B_TXN
Pin #18

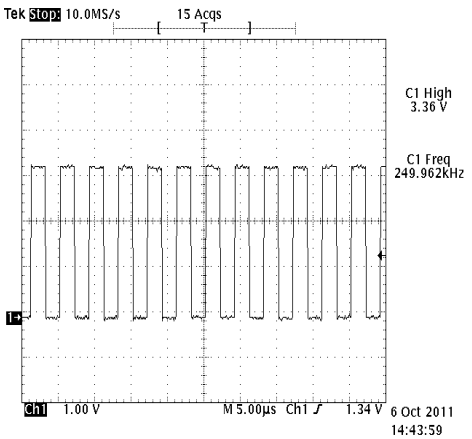
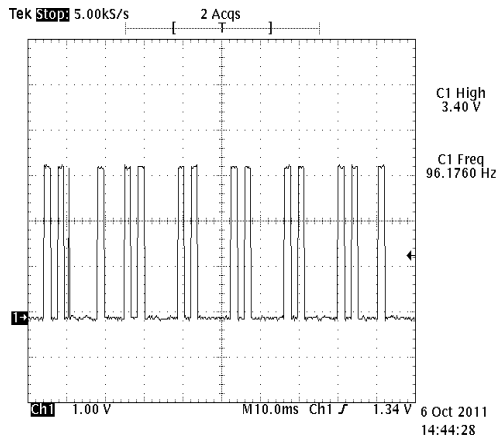
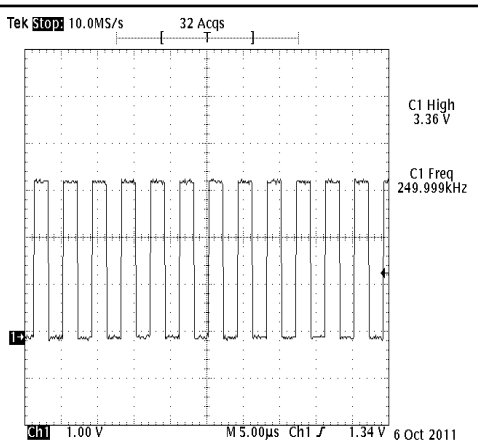
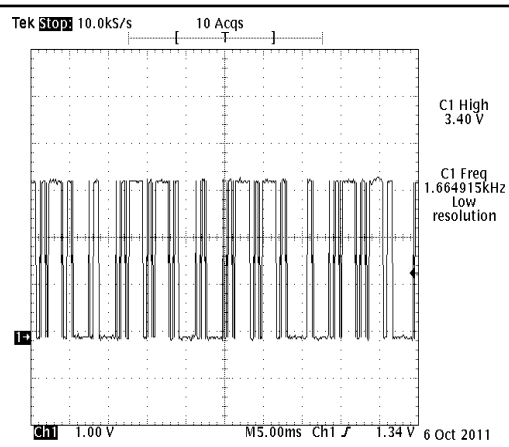
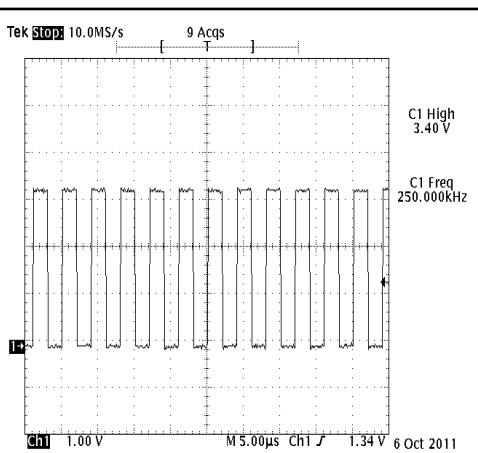
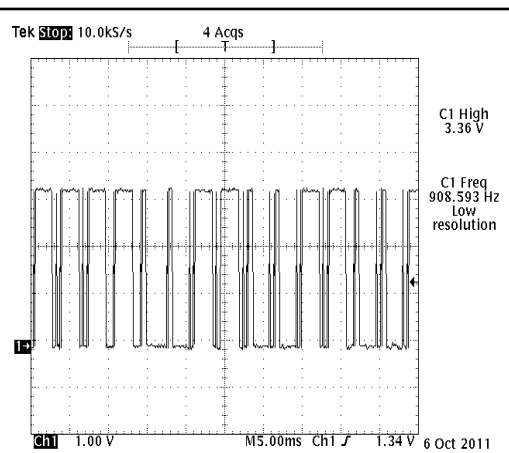


B_RXP
Pin #20

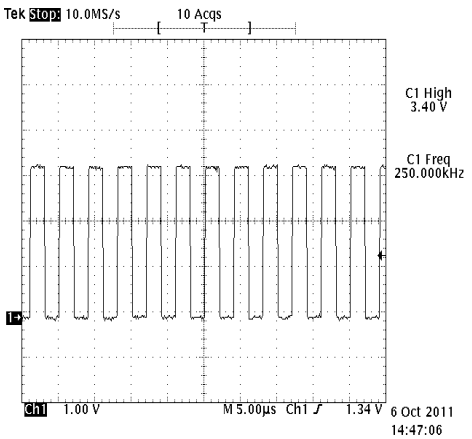
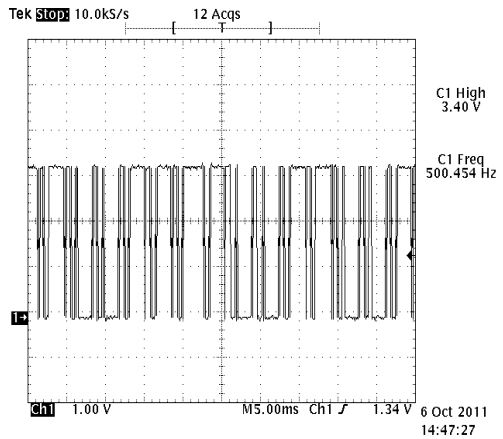
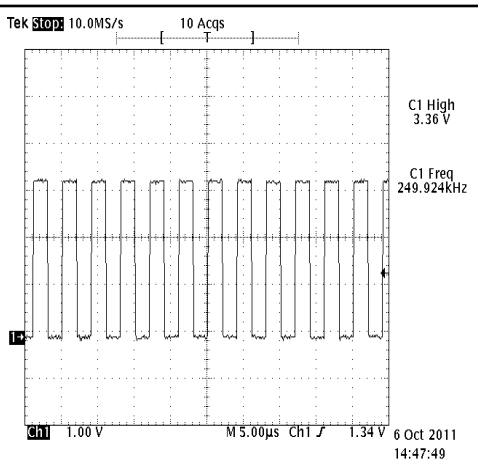
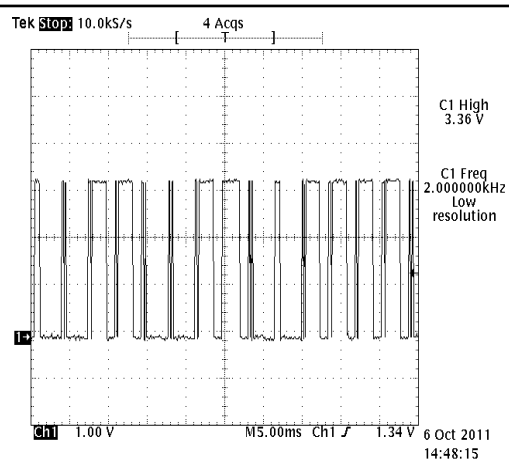
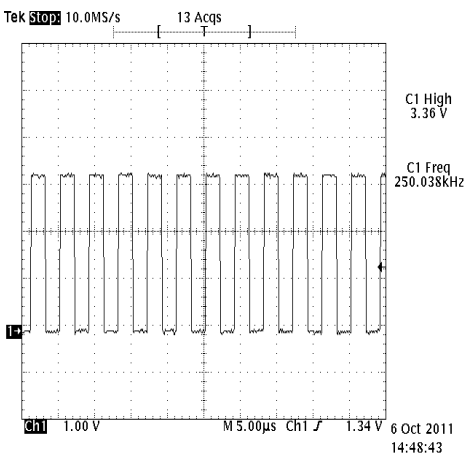
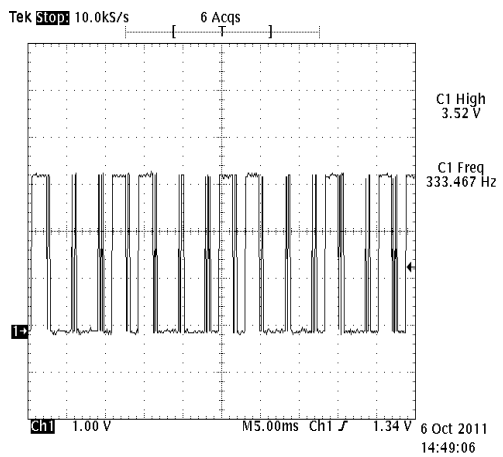


B_RXN
Pin #21

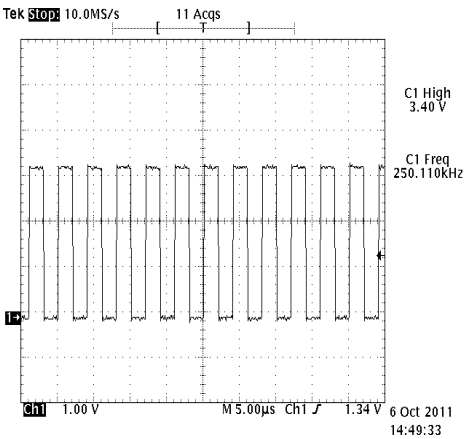
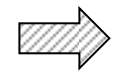
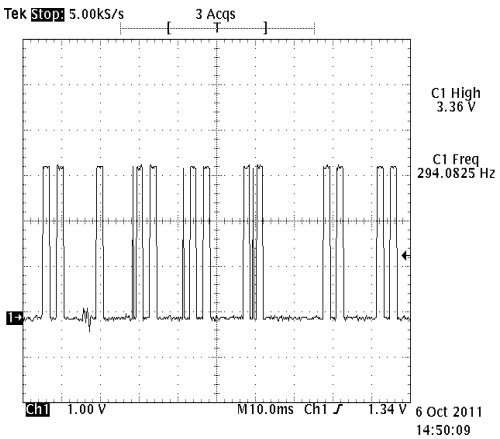
2. Output signal (cont'd)

	B_DATA3 Pin #35		B_DATA3 Pin #35
	B_DATA4 Pin #36		B_DATA4 Pin #36
	B_DATA5 Pin #37		B_DATA5 Pin #37

2. Output signal (cont'd)

	B_DATA6 Pin #38		B_DATA6 Pin #38
	B_DATA7 Pin #39		B_DATA7 Pin #39
	O_INTN Pin #40		O_INTN Pin #40

2. Output signal (cont'd)

	 O_MISO Pin #44		O_MISO Pin #44

World Class Reliability Testing & Failure Analysis Company

Ichon Head Office…….……San 136-1 Ami-ri Bubal-eup Ichon-si Kyoungki-do, 467-701
Tel. 82-31-639-7684, 7617 Fax 82-31-639-7654

Cheongju Branch……..……1 Hyangjeong-dong Hungduk-gu Cheongju-si Chung buk, 361-725
Tel. 82-43-280-2748, 7128 Fax 82-43-280-2653

Gumi Branch……...……171 Imsoo-dong Gumi-si Kyung buk, 730-723
Tel. 82-54-470-1528, Fax 82-54-472-8031

Contact Information (Ichon)
Tel. 82-31-639-7684 (7621)
doseok.ahn@qrtkr.com
dongsung.kim@qrtkr.com