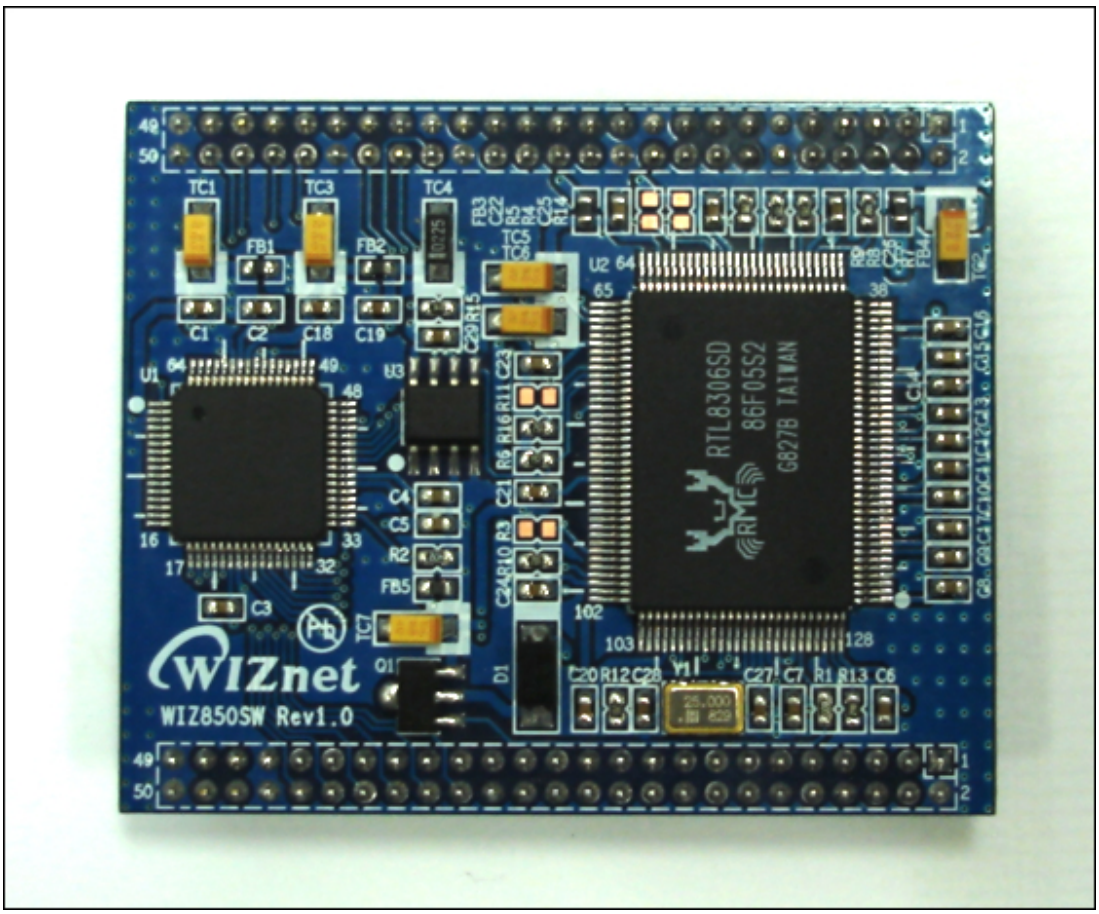
WIZ850SW User Manual

(Ver. 1.0)



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Document History Information

Revision	Data	Description
Ver. 1.0	March 20, 2009	Release with WIZ850SW Launching

WIZnet's Online Technical Support

If you have something to ask about WIZnet Products, Write down your question on Q&A Board in WIZnet website (www.wiznet.co.kr). WIZnet Engineer will give an answer as soon as possible.

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1. Introduction

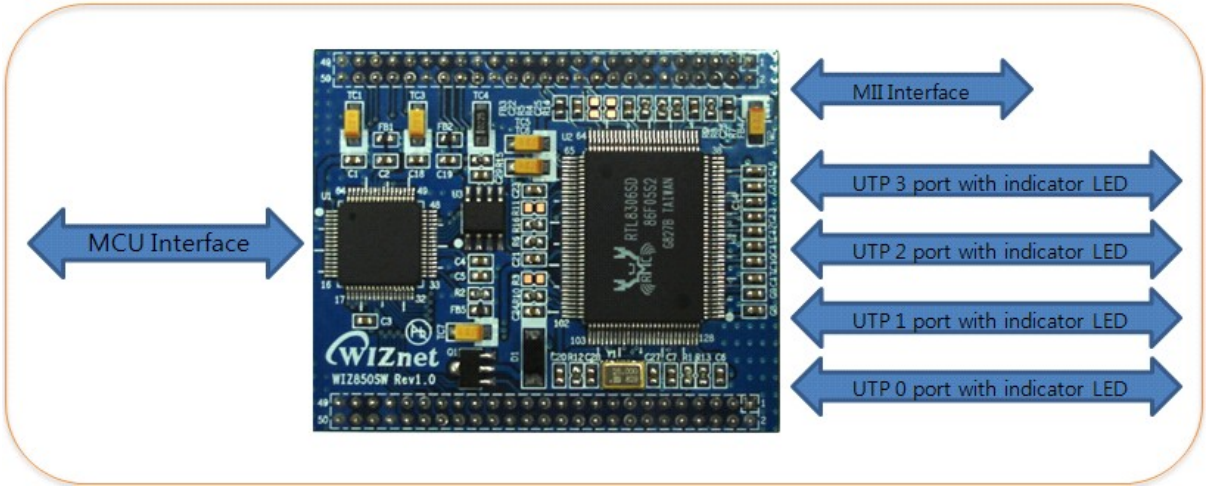
WIZ850SW is the Multi port switching network module that includes W3150A+ (TCP/IP hardwired chip), RTL8306SD(Ethernet switch controller, 6 port, Dual MII), other glue logics.
It can be used as a component and no effort is required to multi port switching.
The WIZ850SW is an ideal option for users who want to develop their multi port Internet enabling systems rapidly.

For the detailed information on implementation of Hardware TCP/IP, refer to the W3150A+ Datasheet.

1.1. Features

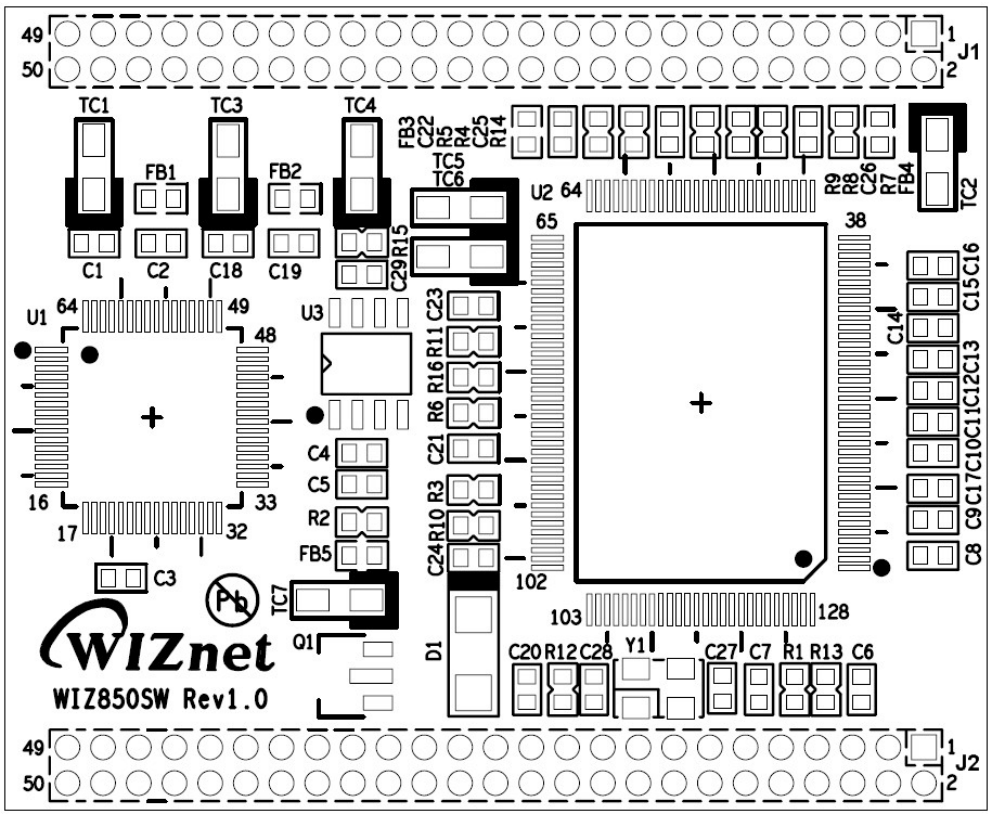
- Supports 10/100 Base TX
- Supports half/full duplex operation
- Supports auto-negotiation and auto cross-over detection
- IEEE 802.3/802.3u Compliance
- Operates 3.3V with 5V I/O signal tolerance
- Supports network status indicator LEDs
- Supports 1 MII interface
- Supports 4 UTP port interface
- Includes Hardware Internet protocols: TCP, IP Ver.4, UDP, ICMP, ARP, PPPoE, IGMP
- Includes Hardware Ethernet protocols: DLC, MAC
- Supports 4 independent connections simultaneously
- Supports MCU bus Interface and SPI Interface
- Supports Direct/Indirect mode bus access
- Supports Socket API for easy application programming
- Interfaces with two 2.00mm pitch 2 x 25 header pin

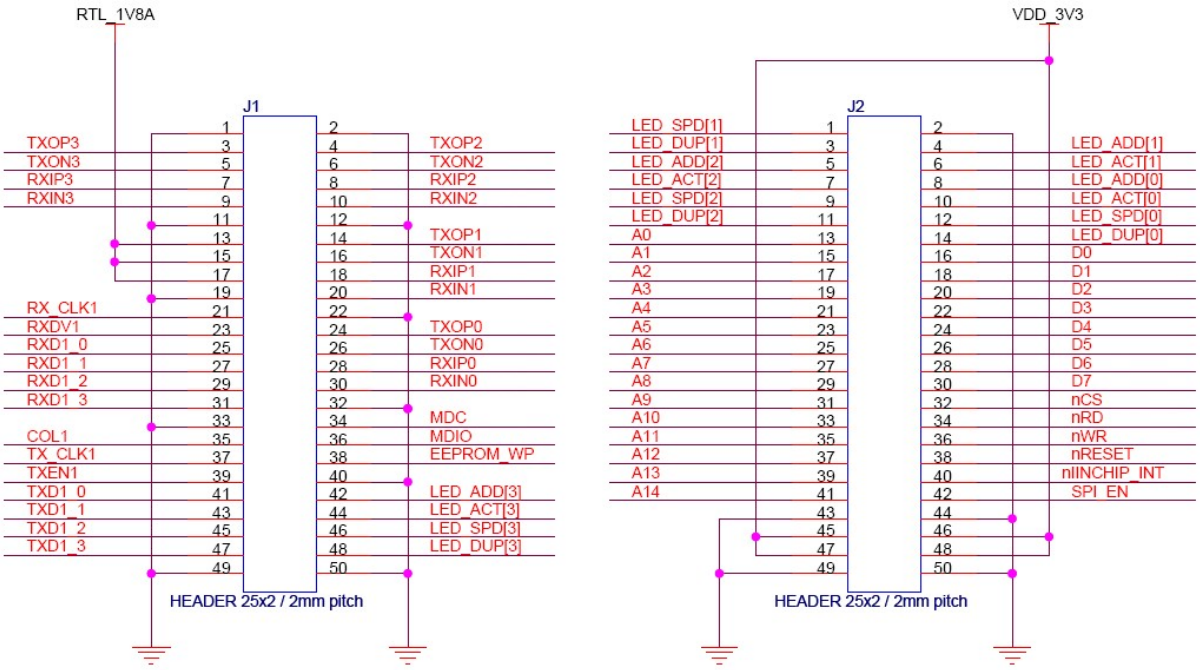
1.2. Block Diagram



2. Pin Assignments & descriptions

2.1. Pin Assignment





I : Input **O : Output**
I/O : Bi-directional Input and output **P : Power**

2.2. Power & Ground

Symbol	Type	Pin No.	Description
RTL_1V8A	**P**	J1:13, J1:15, J1:17	**Power** : 1.8V power output for external transformer
3V3D	**P**	J2:45 J2:46, J2:47, J2:48	**Power** : 3.3 V main power supply
GND	**P**	J1:1, J1:2, J1:11, J1:12, J1:19, J1:22, J1:32, J1:33, J1:40, J1:49, J1:50, J2:2, J2:43, J2:44, J2:49, J2:50	**Ground**

2.3. MCU Interfaces

Symbol	Type	Pin No.	Description
A7 ~ A0	**I**	J2:27, J2:25, J2:23, J2:21, J2:19, J2:17, J2:15, J2:13	**Address** Used as lower address[7…0] pin
A14 ~ A8	**I**	J2:41, J2:39, J2:37, J2:35, J2:33, J2:31, J2:29	**Address** Used as upper address[14…8] pin
D7 ~ D0	**I/O**	J2:30, J2:28, J2:26, J2:24, J2:22, J2:20, J2:18, J2:16	**Data** 8 bit-width data bus[7…0]
nCS	**I**	J2:32	**Module Select** : Active low. nCS of W3150A+
nRD	**I**	J2:34	**Read Enable** : Active low. nRD of W3150A+
nWR	**I**	J2:36	**Write Enable** : Active low nWR of W3150A+
nIINCHIP_INT	**O**	J2:40	**Interrupt** : Active low After reception or transmission it indicates that the W3150A+ requires MCU attention. By writing values to the Interrupt Status Register of W3150A+ the interrupt will be cleared. All interrupts can be masked by writing values to the IMR of W3150A+ (Interrupt Mask Register). For more details refer to the W3150A+ datasheet

2.4. Media Connection Signals

Symbol	Type	Pin No.	Description
RXIP[3:0]	**I**	J1:7, J1:8, J1:18, J1:28	**Differential Receive Data Input.** Each Port support 100Base-TX and 10Base-T
RXIN[3:0]	**I**	J1:9, J1:10, J1:20, J1:30	
TXOP[3:0]	**O**	J1:3, J1:4, J1:14, J1:24	**Differential Transmit Data Output.** Each Port support 100Base-TX and 10Base-T
TXON[3:0]	**O**	J1:5, J1:6, J1:16, J1:26	
RXD1[3:0]	**O**	J1:31, J1:29, J1:27, J1:25	**Receive Data** These are the four parallel receive data lines aligned on the nibble boundaries driven asynchronously to the RXC for reception by the external PHY
RXDV1	**O**	J1:23	**Receive Data Valid** This pin's signal is asserted high when received data is present on the RXD[3:0] lines. The signal is deasserted at the end of the packet. The signal is valid on the rising of the RXC
RX_CLK1	**O**	J1:21	**Receive Clock** This pin provides a continuous clock reference for RXDV and RXD[3:0] signals. RXC is 2.5MHz in the 10Mbps mode, and 25MHz in the 100Mbps mode.
TXD1[3:0]	**I**	J1:47, J1:45, J1:43, J1:41	**Transmit Data** MAC will source TXD[3:0] synchronous with TXC when TXEN is asserted.
TXEN1	**I**	J1:39	**Transmit Enable** The input signal indicates the presence of a valid nibble data on TXD[3:0]
TX_CLK1	**O**	J1:37	**Transmit Clock** This pin provides a continuous clock as a timing reference for TXD[3:0] and TXEN.
COL1	**O**	J1:35	**Collision Detect** COL is asserted high when a collision is detected on the media.

2.5. Miscellaneous Signals

Symbol	Type	Pin No.	Description
nRESET	**I**	J2:38	**Reset :** This pin is active low input to initialize or re-initialize W3150A+. By asserting this pin low for at least 2us, all internal registers will be re-initialized to their default states.
SPI_EN	**I**	J2:42	**SPI Interface Enable** This active high pin selects enable / disable of the W3150A+'s SPI mode. This pin is internally pulled down. If this signal is high then SPI mode is enabled.
EEPROM_WP	**I**	J1:38	**Write Protect** This active high pin protect a write operation of the external EEPROM. Please do not use this signal for general applications.
MDC	**I**	J1:34	**Management Data Clock** This pin is for RTL8306SD. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 2.5MHz. Please do not use this signal for general applications.
MDIO	**I/O**	J1:36	**Management Data Input / Output** This pin is for RTL8306SD. This pin provides the bi-directional signal used to transfer management information. Please do not use this signal for general applications.

2.6. Network status indicator LED Signals

Each port has four LED indicator pins. Each pin may have different indicator meanings as set by pins LEDMODE[1:0]. WIZ850SW's default setting is LEDMODE[1:0] = 11. (refer to the schematic).

Symbol	Type	Pin No.	Description
LED_ACT[3:0]	**O**	J1:44, J2:7, J2:6, J2:10	**Active LED** LEDMODE[1:0]=11 : Link/Act (On=Link, Off=No Link, Flash=Tx or Rx activity) LEDMODE[1:0]=10 : Act (Off=No activity, Flash=Tx or Rx activity) LEDMODE[1:0]=01 : RxAct (Off=No activity, Flash=Rx activity) LEDMODE[1:0]=00 : Link/Act (On=Link, Off=No Link, Flash=Tx or Rx activity)
LED_SPD[3:0]	**O**	J1:46, J2:9, J2:1, J2:12	**Speed LED** LEDMODE[1:0]=11 : Speed (On=100, Off=10) LEDMODE[1:0]=10 : Speed (On=100, Off=10) LEDMODE[1:0]=01 : Speed (On=100, Off=10) LEDMODE[1:0]=00 : Speed (On=100, Off=10)
LED_DUP[3:0]	**O**	J1:48, J2:11, J2:3, J2:14	**Duplex LED** LEDMODE[1:0]=11 : Duplex/Col (On=Full, Off=Half with no collision, Flash=Collision) LEDMODE[1:0]=10 : Duplex/Col (On=Full, Off=Half with no collision, Flash=Collision) LEDMODE[1:0]=01 : TxAct (Off=No activity, Flash=Tx activity) LEDMODE[1:0]=00 : Col (On=Collide, Off=Half with no collision)
LED_ADD[3:0]	**O**	J1:42, J2:5, J2:4, J2:8	**Additional LED** LEDMODE[1:0]=11 : Link/Act/Speed (On for link established. Blinking every 43ms when the corresponding port is transmitting or reseiving at 100Mbps. Blinking every 120ms when the corresponding port is transmitting or reseiving at 10Mbps.) LEDMODE[1:0]=10 : Bi-color Link/Act LEDMODE[1:0]=01 : Link (Off=Link, Off=No Link) LEDMODE[1:0]=00 : Duplex (On=Full, Off=Half)

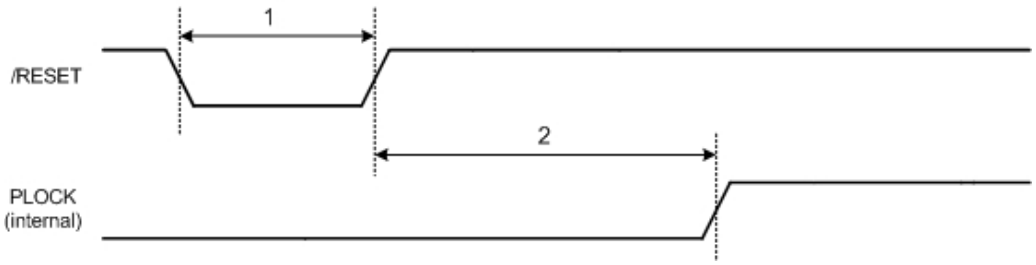
3. Timing Diagrams

WIZ850SW provides following interfaces of W3150A+.

-. Direct/Indirect mode bus access

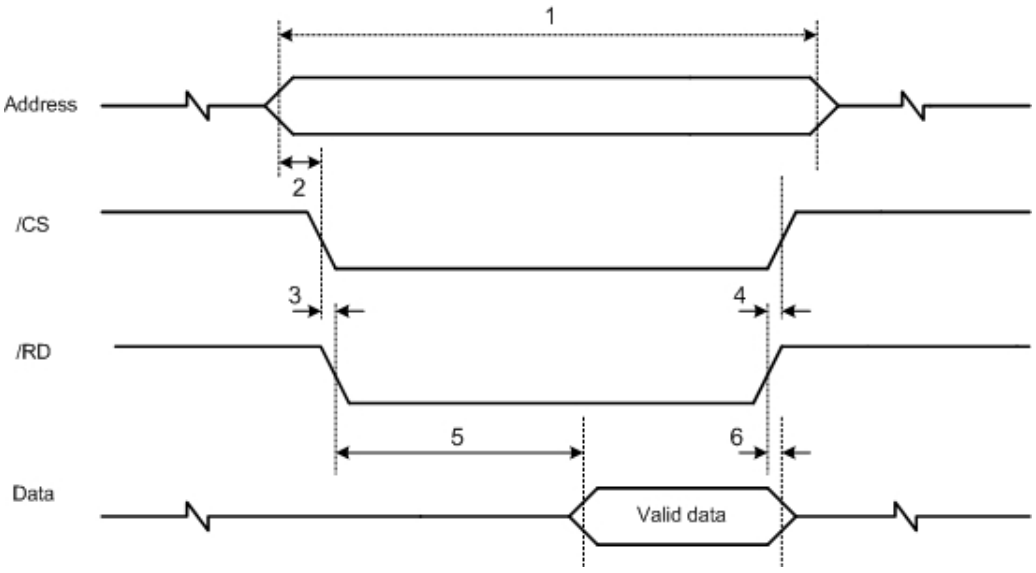
-. SPI access

3.1. Reset Timing



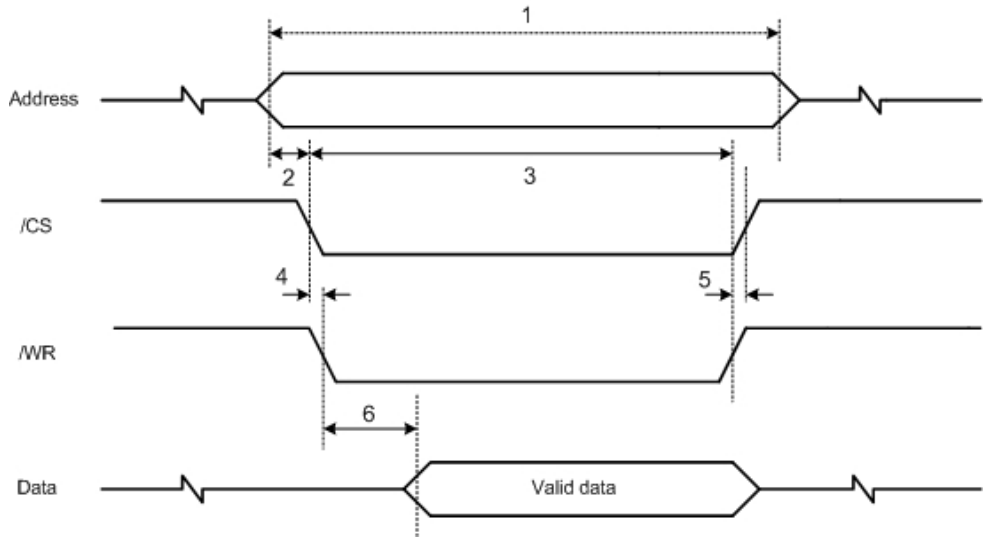
	Description	Min	Max
1	Reset Cycle Time	2 us	-
2	/RESET to internal PLOCK	-	10 ms

3.2. Register/Memory READ Timing



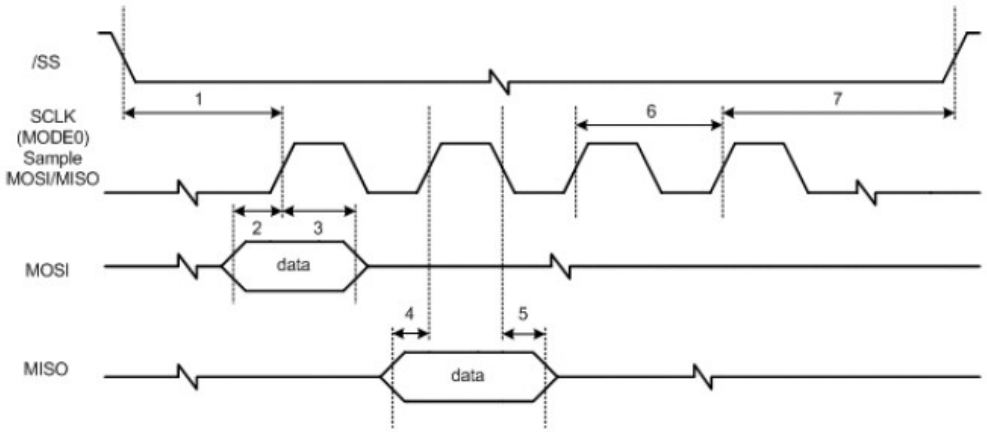
	Description	Min	Max
1	Read Cycle Time	80 ns	-
2	Valid Address to /CS low time	8 ns	-
3	/CS low to /RD low time	-	1 ns
4	/RD high to /CS high time	-	1 ns
5	/RD low to Valid Data Output time	-	80 ns
6	/RD high to Data High-Z Output time	-	1 ns

3.3. Register/Memory WRITE Timing



	Description	Min	Max
1	Write Cycle Time	70 ns	-
2	Valid Address to /CS low time	7 ns	-
3	/CS low to /WR high time	70 ns	-
4	/CS low to /WR low time	-	1 ns
5	/WR high to /CS high time	-	1 ns
6	/WR low to Valid Data time	-	14 ns

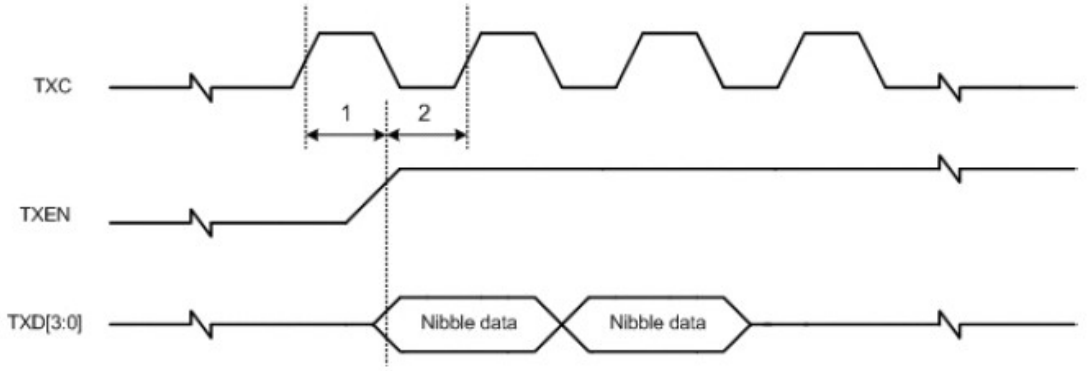
3.4. SPI Timing



	Description	Mode	Min	Max
1	/SS low to SCLK	Slave	21 ns	-
2	Input setup time	Slave	7 ns	-
3	Input hold time	Slave	28 ns	-
4	Output setup time	Slave	7 ns	14 ns
5	Output hold time	Slave	21 ns	-
6	SCLK time	Slave	70 ns	-
7	SCLK high to /SS high	Slave	21ns	-

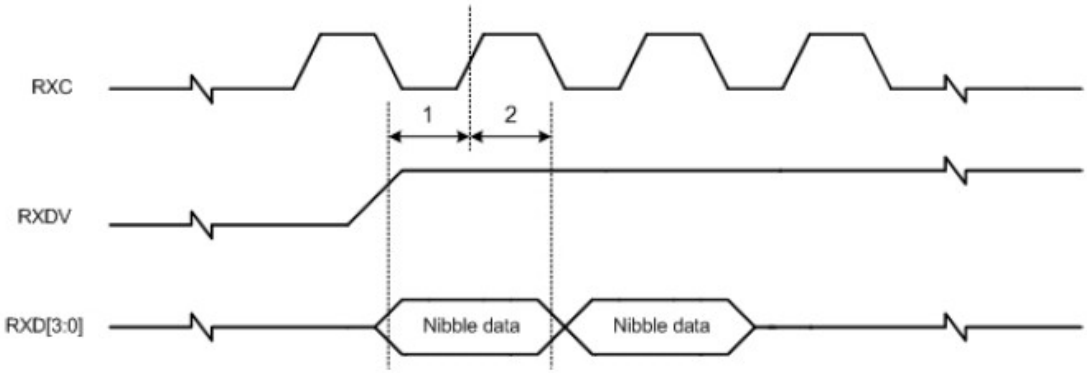
3.5. MII(Media Independent Interface) Timing

■ MII Tx TIMING



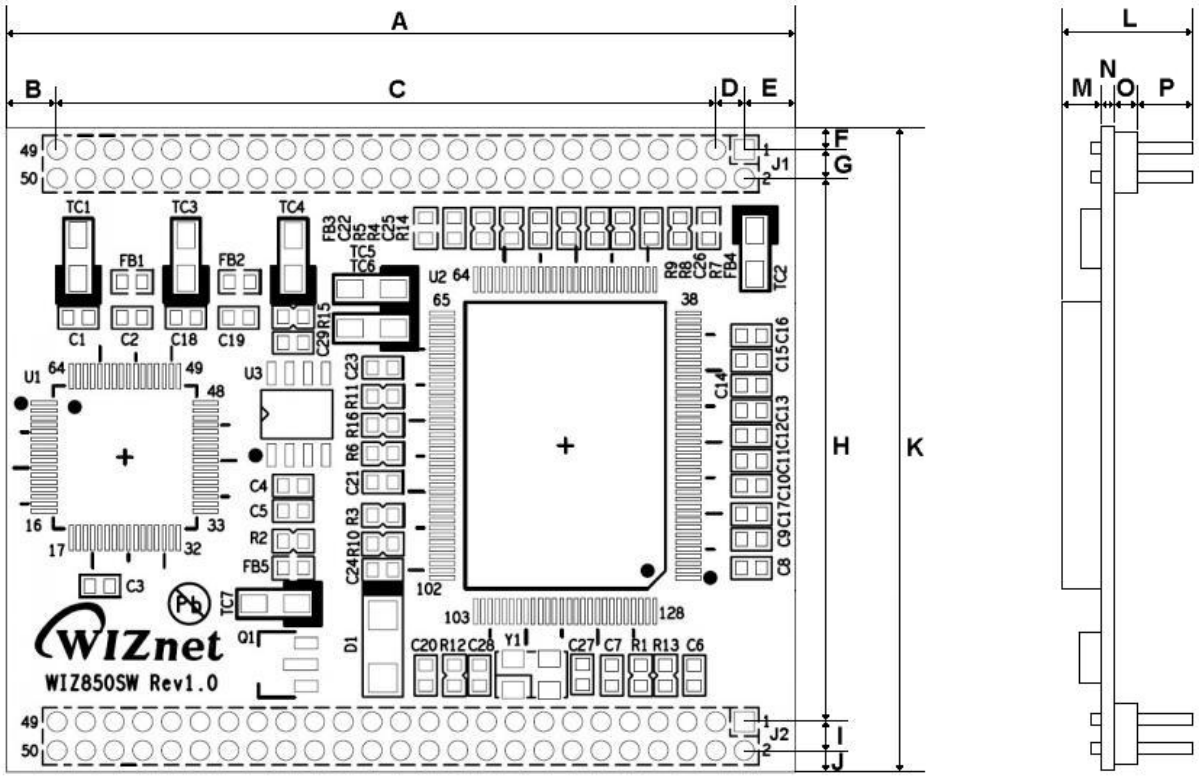
	Description	Note	Min	Max
1	TX_CLK to TXD, TXEN	10Mbps	201 ns	205 ns
2	TXD, TXEN setup time to TX_CLK	10Mbps	195 ns	198 ns
1	TX_CLK to TXD, TXEN	100Mbps	22 ns	25 ns
2	TXD, TXEN setup time to TX_CLK	100Mbps	15 ns	18 ns

■ MII Rx TIMING



	Description	Note	Min	Max
1	Valid data to RX_CLK time (setup time)	10Mbps	5 ns	-
2	RX_CLK to valid data time (hold time)	10Mbps	5 ns	-
1	Valid data to RX_CLK time (setup time)	100Mbps	5 ns	-
2	RX_CLK to valid data time (hold time)	100Mbps	5 ns	-

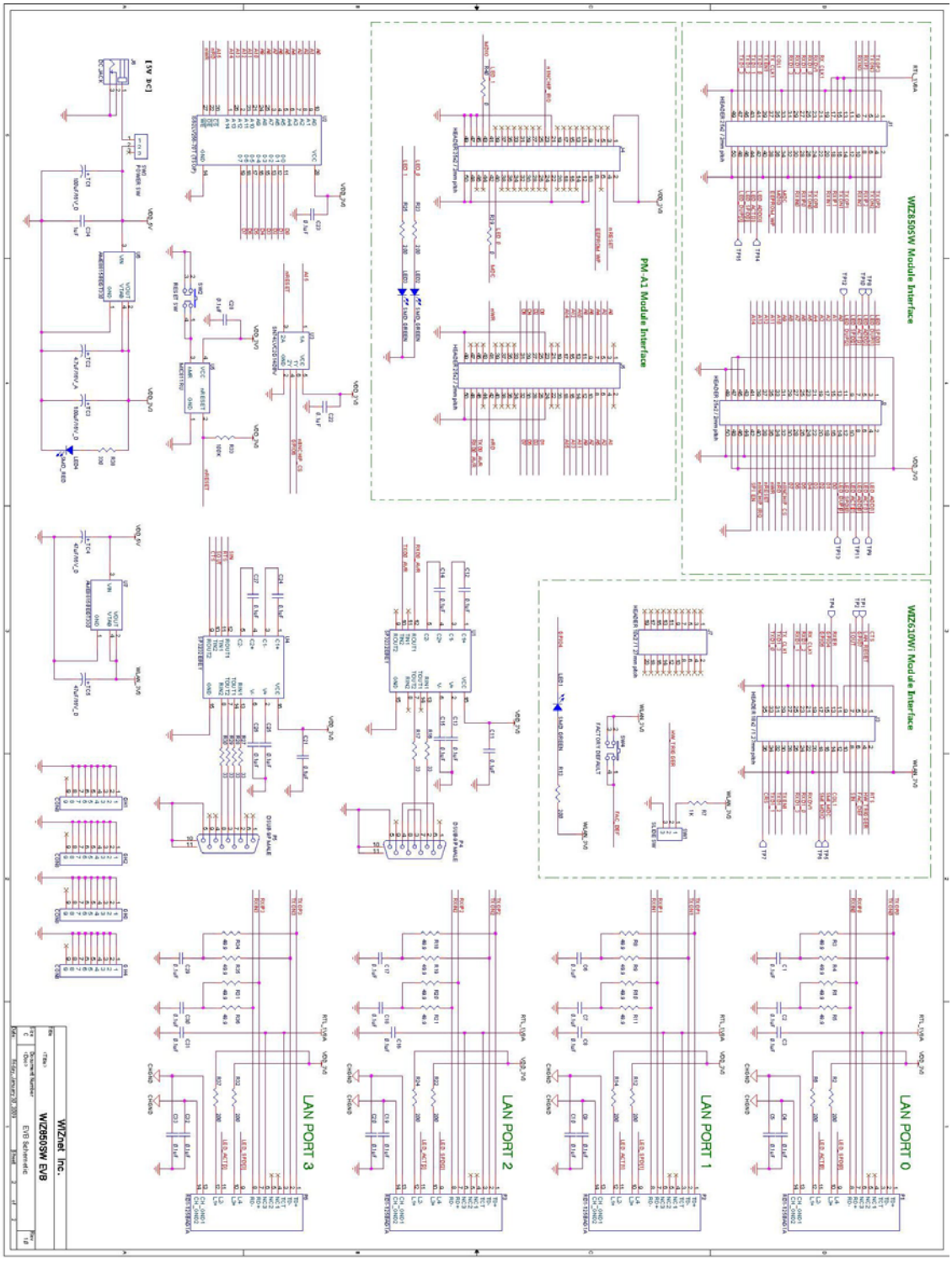
4. Dimensions



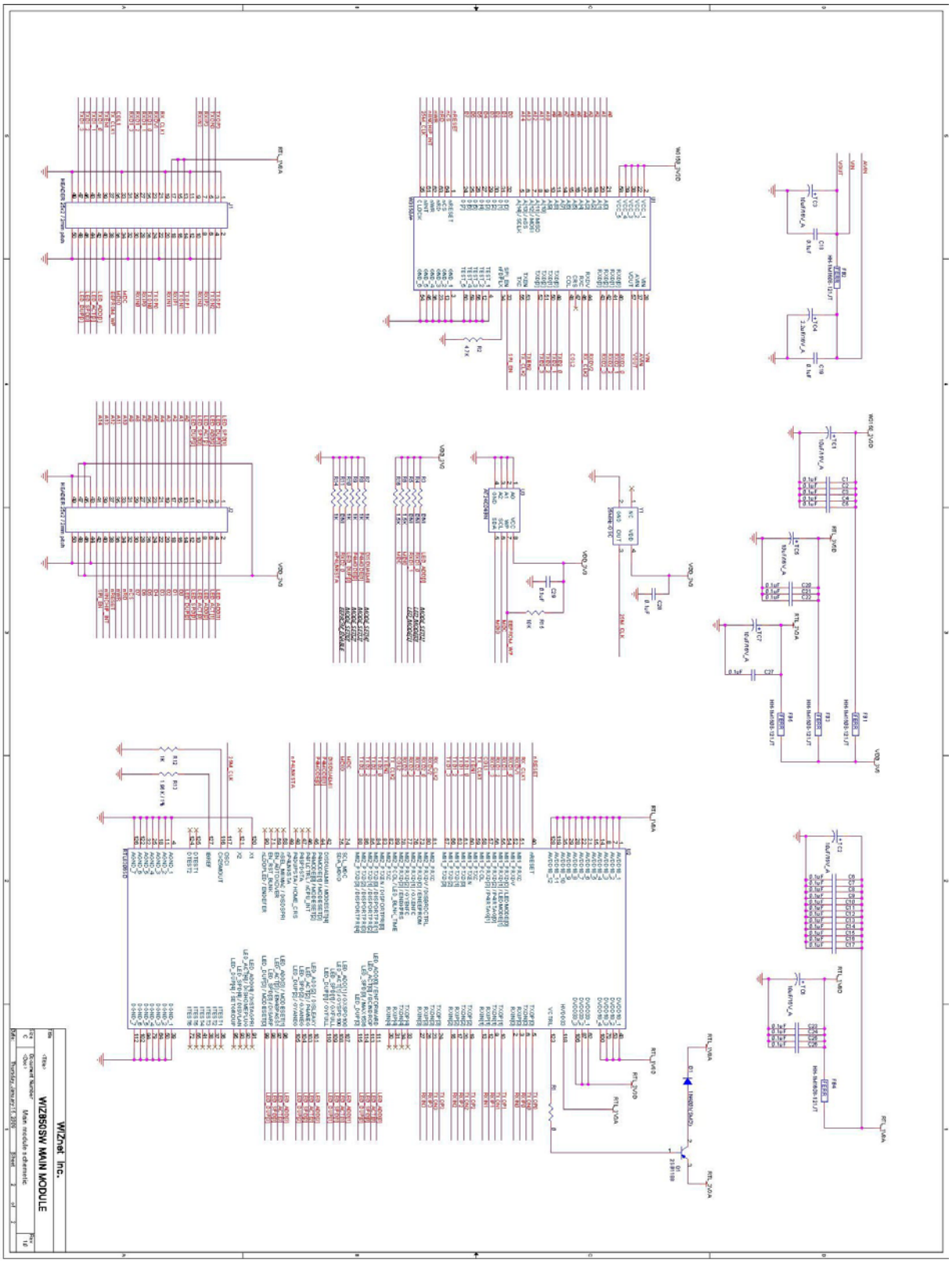
Symbols	Dimensions (mm)
A	55.0
B	3.5
C	46.0
D	2.0
E	3.5
F	1.5
G	2.0
H	38.0
I	2.0
J	1.5
K	45.0
L	10.5
M	3.4
N	1.6
O	2.0
P	3.5

5. Design Guide

5.1. Reference Board Schematic



5.2. WIZ850SW Module Schematic



6. Partlist

Item	Q.ty	Reference	Part	Tech. Characteristics	Package
1	29	C1,C2,C3,C4, C5,C6,C7,C8, C9,C10,C11, C12,C13,C14, C15,C16,C17, C18,C19,C20, C21,C22,C23, C24,C25,C26, C27,C28,C29	0.1uF	50V-20% Ceramic	CASE 0603
2	6	TC1,TC2,TC3, TC5,TC6,TC7	10uF / 16V_A	16Vmin 10%	EIA/IECQ 3216
3	1	TC4	2.2uF / 16V_A	16Vmin 10%	EIA/IECQ 3216
4	1	D1	1N4001 (SMA size)	1A Rectifier Diode	DO-214AC
5	5	FB1,FB2,FB3, FB4,FB5	HH-1M1608-121JT	Chip Ferrite BEAD	CASE 0603
6	2	J1,J2	25x2 50pin-Header	2.00mm pitch PIN-Header (Male)	DIP (2.00MM)
7	1	Q1	2SB1188	PNP Power Transister	SC-62
8	1	R1	0	1/10W-5% SMD	CASE 0603
9	1	R2	4.7K	1/10W-5% SMD	CASE 0603
10	2	R6,R16	1.5K	1/10W-5% SMD	CASE 0603
11	6	R7,R8,R9,R10, R12,R14	1K	1/10W-5% SMD	CASE 0603
12	1	R13	1.96K / 1%	1/10W-1% SMD	CASE 0603
13	1	R15	10K	1/10W-5% SMD	CASE 0603
14	1	U1	W3150A+	WIZnet Hardware TCP/IP	LQFP64
15	1	U2	RTL8306SD	Realtek Ethernet switch controller	PQFP128
16	1	U3	AT24C04BN	Serial EEPROM	SOIC8
17	1	Y1	25MHz Oscillator	Oscillator SMD type	SCO-53
18	1		WIZ850SW REV1.0 1.6T 4LAYER	PRINTED CIRCUIT BOARD	

7. Warranty

WIZnet Co., Ltd offers the following limited warranties applicable only to the original purchaser. This offer is non-transferable.

WIZnet warrants our products and its parts against defects in materials and workmanship under normal use for period of standard ONE(1) YEAR for the WIZ850SW and labor warranty after the date of original retail purchase. During this period, WIZnet will repair or replace a defective products or part free of charge.

Warranty Conditions:

1. The warranty applies only to products distributed by WIZnet or our official distributors.
2. The warranty applies only to defects in material or workmanship as mentioned above in 7.Warranty. The warranty applies only to defects which occur during normal use and does not extend to damage to products or parts which results from alternation, repair, modification, faulty installation or service by anyone other than someone authorized by WIZnet Inc. ; damage to products or parts caused by accident, abuse, or misuse, poor maintenance, mishandling, misapplication, or used in violation of instructions furnished by us ; damage occurring in shipment or any damage caused by an act of God, such as lightening or line surge.

Procedure for Obtaining Warranty Service

1. Contact an authorized distributors or dealer of WIZnet Inc. for obtaining an RMA (Return Merchandise Authorization) request form within the applicable warranty period.
2. Send the products to the distributors or dealers together with the completed RMA request form. All products returned for warranty must be carefully repackaged in the original packing materials.
3. Any service issue, please contact to sales@wiznet.co.kr