W7200 Datasheet

Version 1.1.0

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1 Introduction

iMCU W7200 is the one-chip solution which integrates an Cortex-M3 core, 20KB SRAM and hardwired TCP/IP Core for high performance and easy development.

The TCP/IP core is a market-proven hardwired TCP/IP stack with an integrated Ethernet MAC & PHY. The Hardwired TCP/IP stack supports the TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE which has been used in various applications for years.

2 Device Overview

2.1.1 W7200 Features

- ARM 32-bit Cortex-M3 Core from STmicro
  - 72MHz maximum frequency (1.25 DMIPS/MHz)
  - 20KBytes Data Memory (RAM)
  - 128KBytes Code Memory
  - Low Power: Support Sleep, Stop and Standby modes
  - 7 timers
    . Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
    . 2 watchdog timers (Independent and Window)
    . SysTick timer 24-bit downcounter
  - Full-duplex UART
  - Programmable Watchdog Timer
  - CRC calculation unit, 96-bit unique ID
  - GPIO, 12bits ADC, CAN, I2C, SPI, USART and USB Interfaces

- Hardwired TCP/IP
  - 10BaseT/100BaseTX Ethernet PHY embedded
  - Power down mode supported for saving power consumption
  - Hardwired TCP/IP Protocols: TCP, UDP, ICMP, IPv4 ARP, IGMP, PPPoE, Ethernet
  - Auto Negotiation (Full-duplex and half duplex), Auto MDI/MDIX
  - ADSL connection with PPPoE Protocol with PAP/CHAP Authentication mode support
  - 8 independent sockets which are running simultaneously
  - 32Kbytes Data buffer for the Network
  - Network status LED outputs (TX, RX, Full/Half duplex, Collision, Link, and Speed)
  - Not supports IP fragmentation

2.1.2 W7200 Block Diagram & Features

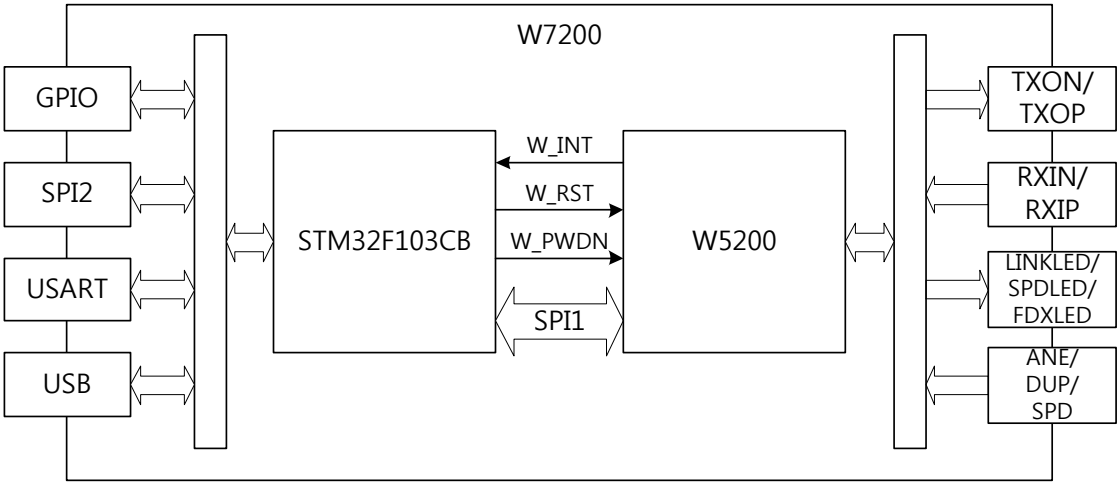


Figure 1 W7200 Block Diagram

The W7200 internal block diagram is shown in the Figure 1. W7200 is implemented by STM32F103CB and W5200. STM32F103CB provides GPIO, I2C, SPI, USB and USART. W5200 provides TCP/IP Stack, MAC and Ethernet PHY. STM32F103CB and W5200 are wired by SPI of STM32F103CB.

2.1.2.1 MCU

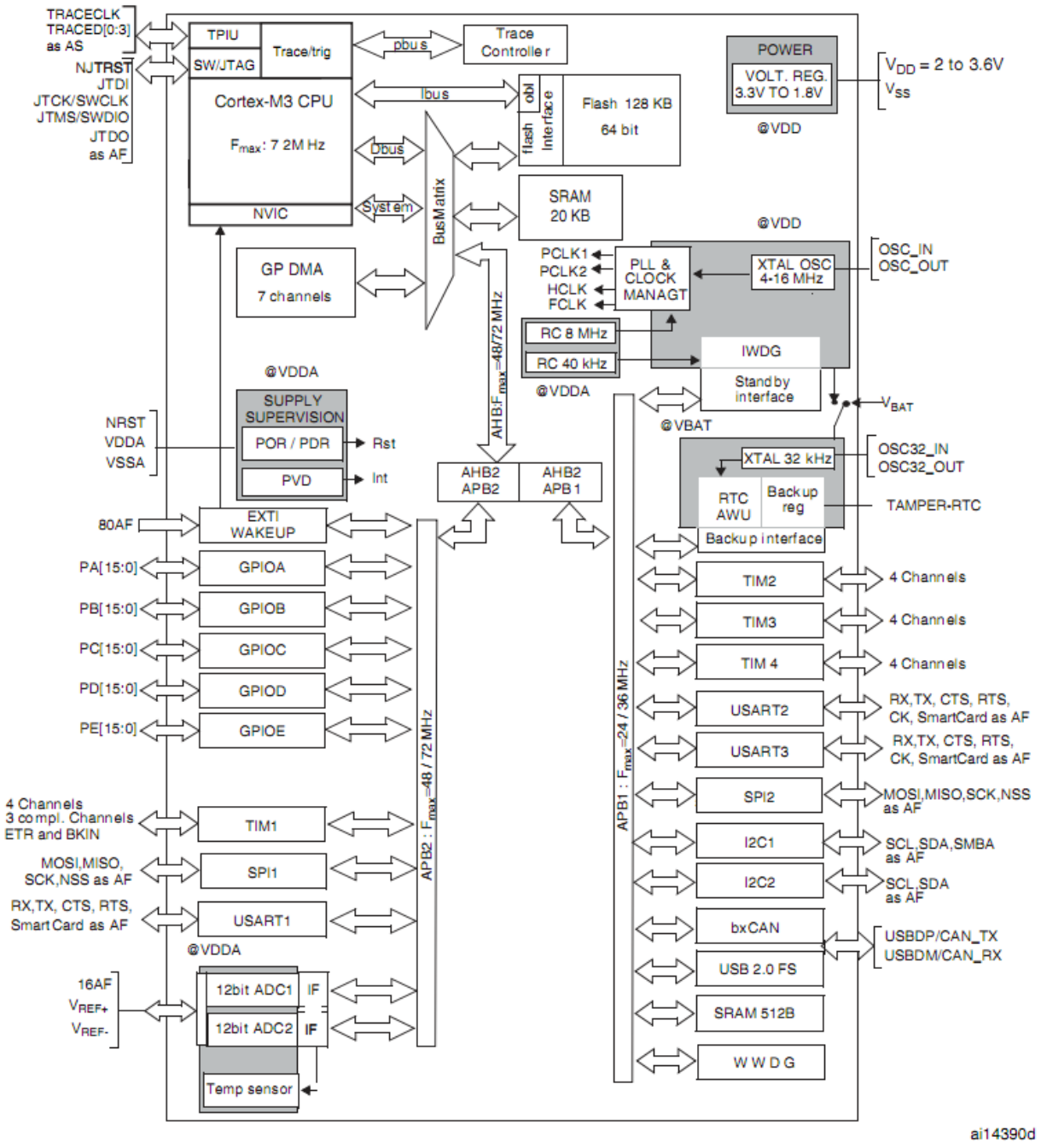


Figure 2 STM32F103xx Performance Line Block Diagram

The ARM Cortex™-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F103xx performance line family having an embedded ARM core, is therefore compatible with all ARM tools and software.

Figure 2 shows the general block diagram of the device family

2.1.2.2 TCP/IP Core

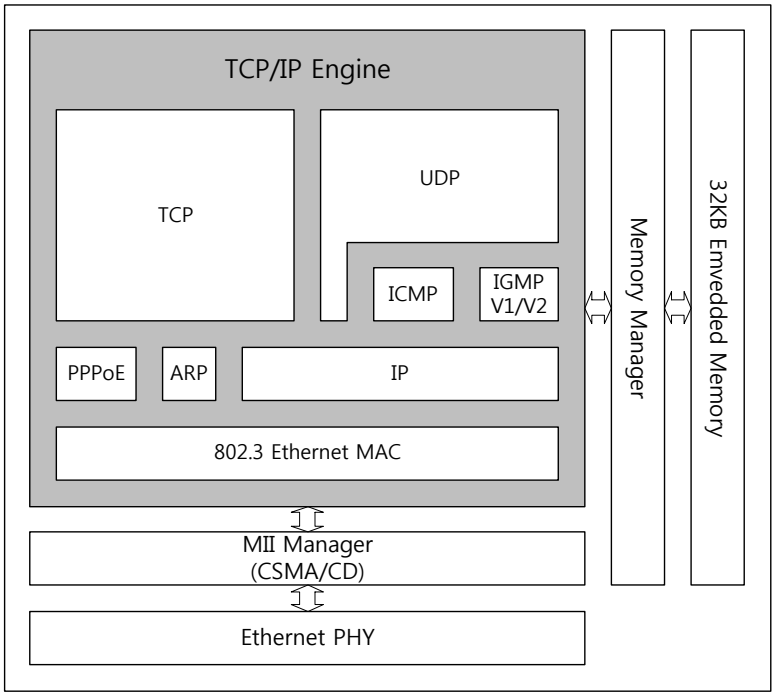


Figure 3 TCP/IP Core Block Diagram

The TCP/IP Core is composed of a fully hardwired market-proven TCP/IP stack and an integrated Ethernet MAC & PHY. Hardwired TCP/IP stack supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE, which has been proven in various applications for many years.

TCP/IP Core uses a 32Kbytes internal buffer as its data communication memory. By using W5200, users can implement the Ethernet application they need by using a simple socket program instead of handling a complex Ethernet Controller.

In order to reduce power consumption of the system, TCP/IP Core provides WOL (Wake on LAN) and power down mode. To wake up during WOL, TCP/IP Core should be received magic packet, which is the Raw Ethernet packet.

TCP/IP Engine

TCP/IP Engine is a hardwired logic based network protocol which contains technology of WIZnet.

- TCP(Transmission Control Protocol)

This protocol operates in the TCP layer and provides data communication. Both TCP server and client modes are supported.

- UDP(User Datagram Protocol)

It is a protocol which supports data communication at the UDP layer. User datagram such as unicast, multicast, and broadcast are supported

- ICMP(Internet Control Message Protocol)

ICMP is a protocol which provides information, unreachable destination. When a Pingrequest ICMP packet is received, a Ping-reply ICMP packet is sent.

- IGMPv1/v2(Internet Group Management Protocol version 1/2)

This protocol processes IGMP messages such as the IGMP Join/Leave. The IGMP is only enabled in UDP multicast mode. Only version 1 and 2 of IGMP logic is supported. When using a newer version of IGMP, IGMP should be manually implemented in the IP layer.

- PPPoE(Point-To-Point Protocol over Ethernet)

This protocol uses PPP service over Ethernet. The payload (PPP frame) is encapsulated inside an Ethernet frame during a transmission. When receiving, it de-capsulates the PPP frame. PPPoE supports PPP communication with PPPoE server and PAP/CHAP authentications.

- ARP(Address Resolution Protocol)

ARP is the MAC address resolution protocol by using IP address. This protocol exchanges ARP-reply and ARP-request from peers to determine the MAC address of each other

- IP (Internet Protocol)

This protocol operates in the IP layer and provides data communication. IP fragmentation is not supported. It is not possible to receive the fragmented packets. All protocol number is supported except for TCP or UDP. In case of TCP or UDP, use the hardwired embedded TCP/IP stack.

- 802.3 Ethernet MAC(Media Access Control)

This controls Ethernet access of CSMA/CD(Carrier Sense Multiple Access with Collision Detect). The protocol is based on a 48-bit source/destination MAC address.

Ethernet PHY

The W7200 includes 10BaseT/100BaseTX Ethernet PHY. It supports half-duplex/full-duplex, auto-negotiation and auto-MDI/MDIX. It also supports 6 network indicator LED outputs such as

Link, TX, RX status, Collision, speed and duplex.

2.1.3 Pin Description

2.1.3.1 Pin Layout

Package type: LGA 60

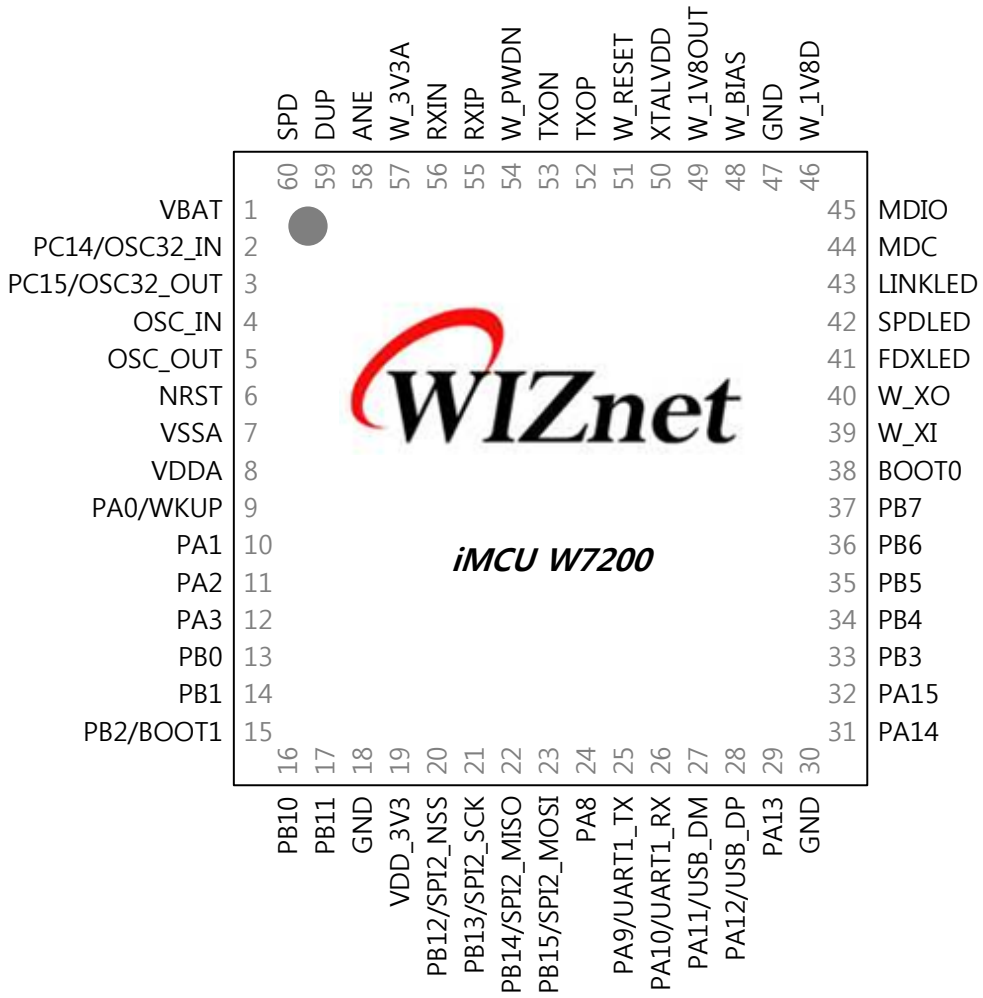


Figure 4 W7200 LGA60 Pin Layout

2.1.3.2 Pin Definitions

Pins	Pin name	Type	Main functions	Alternate functions	
				Default	Remap
1	VBAT	S	VBAT		
2	PC14/OSC32_IN	I/O	PC14	OSC32_IN	
3	PC15/OSC32_OUT	I/O	PC15	OSC32_OUT	
4	OSC_IN	I	OSC_IN		
5	OSC_OUT	O	OSC_OUT		
6	NRST	I/O	NRST		
7	VSSA	S	VSSA		
8	VDDA	S	VDDA		
9	PA0/WKUP	I/O	PA0	WKUP/ USART2_CTS/ ADC12_IN0/ TIM_CH1_ETR	
10	PA1	I/O	PA1	USART2_RTS/ ADC12_IN1/ TIM_CH2	
11	PA2	I/O	PA2	USART2_TX/ ADC12_IN2/ TIM_CH3	
12	PA3	I/O	PA3	USART2_RX/ ADC12_IN3/ TIM_CH4	
13	PB0	I/O	PB0	ADC12_IN8/ TIM3_CH3	TIM1_CH2N
14	PB1	I/O	PB1	ADC12_IN9/ TIM3_CH4	TIM1_CH3N
15	PB2/BOOT1	I/O	PB2/BOOT1		
16	PB10	I/O	PB10	I2C2_SCL/ USART3_TX	TIM2_CH3
17	PB11	I/O	PB11	I2C2_SDA/ USART3_RX	TIM2_CH4
18	GND		GND		
19	VDD_3V3	S	VDD_3V3		

Pins	Pin name	Type	Main functions	Alternate functions	
				Default	Remap
20	PB12/ SPI2_NSS	I/O	PB12	SPI2_NSS/ I2C2_SMBAI/ USART3_CK/ TIM1_BKIN	
21	PB13/ SPI2_SCK	I/O	PB13	SPI2_SCK/ USART3_CTS/ TIM1_CH1N	
22	PB14/ SPI2_MISO	I/O	PB14	SPI2_MISO/ USART3_RTS/ TIM1_CH2N	
23	PB15/ SPI2_MOSI	I/O	PB15	SPI2_MOSI/ TIM1_CH3N	
24	PA8	I/O	PA8	USART1_CK/ TIM1_CH1/MCO	
25	PA9/ UART1_TX	I/O	PA9	UART1_TX/ TIM1_CH2	
26	PA10/ UART1_RX	I/O	PA10	UART1_RX/ TIM1_CH3	
27	PA11/ USB_DM	I/O	PA11	UART1_CTS/ CANRX/ USBDM/ TIM1_CH4	
28	PA12/ USB_DP	I/O	PA12	UART1_RTS/ CANTX/ USBDP/ TIM1_ETR	
29	PA13	I/O	JTMS/SWDIO		PA13
30	GND		GND		
31	PA14	I/O	JTCK/SWCLK		PA14
32	PA15	I/O	JTDI		TIM2_CH1_ETR/ PA15/SPI1_NSS
33	PB3	I/O	JTDO		TIM2_CH2/PB3/ TRACESWO/ SPI1_SCK

Pins	Pin name	Type	Main functions	Alternate functions	
				Default	Remap
34	PB4	I/O	JNTRST		TIM3_CH1/ PB4/SPI1_MISO
35	PB5	I/O	PB5	I2C1_SMBAI	TIM3_CH2/ SPI1_MOSI
36	PB6	I/O	PB6	I2C1_SCL/ TIM4_CH1	USART1_TX
37	PB7	I/O	PB7	I2C1_SDA/ TIM4_CH2	USART1_RX
38	BOOT0	I	BOOT0		
39	W_XI	I	25MHz input		
40	W_XO	O	25MHz output		
41	FDXLED	O	Full Duplex/ Collision LED		
42	SPDLED	O	Link speed LED		
43	LINKLED	O	Link LED		
44	RSV	-	These pins are should be pull-up.		
45	RSV	-			
46	W_1V8D	S	W_1V8D		
47	GND		GND		
48	W_BIAS	O	W_BIAS		
49	W_1V8OUT	O	W_1V8OUT		
50	XTALVDD	I	XTALVDD		
51	W_RESET	I	W_RESET		
52	TXOP	O	TXOP/TXON Signal Pair		
53	TXON	O			
54	W_PWDN	I	W_PWDN		
55	RXIP	I	RXIP/RXIN Signal Pair		
56	RXIN	I			
57	W_3V3A	S	W_3V3A		
58	ANE	I	Auto Negotiation Mode Enable		
59	DUP	I	Full Duplex Mode Enable		
60	SPD	I	Speed Mode		

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	DC Supply voltage	-0.5 to 3.63	V
V_{IN}	DC input voltage	-0.5 to 5.5 (5V tolerant)	V
I_{IN}	DC input current	5	mA
T_{OP}	Operating temperature	-40 to 85	°C
T_{STG}	Storage temperature	-55 to 125	°C

***COMMENT**: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage.

3.2 DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD	DC Supply voltage	Junction temperature is from -55°C to 125°C	2.97		3.6	V
VIH	High level input voltage		2.0		5.5	V
VIL	Low level input voltage		0.3		0.8	V
VOH	High level output voltage		2.4			V
VOL	Low level output voltage				0.4	V
II	Input Current	VIN = VDD			5	μA

3.3 POWER DISSIPATION(Vcc 3.3V Temperature 25°C)

Condition	Min	Typ	Max	Unit
100M Link	-	200	215	mA
10M Link	-	147	162	mA
Loss Link	-	158	173	mA
100M Transmitting	-	200	215	mA
10M Transmitting	-	147	162	mA
Power Down mode	-	37	39	mA

3.4 AC Characteristics

3.4.1 W_Reset Timing

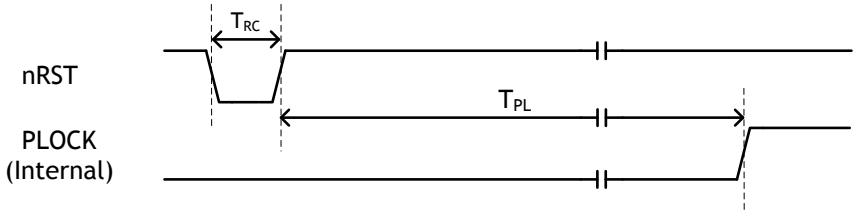


Figure 5 Reset Timing

Symbol	Description	Min	Max
TRC	Reset Cycle Time	2 us	-
TPL	nRST internal PLOCK	-	150 ms

3.4.2 Crystal Characteristics

3.4.2.1 W5200_OSC

Parameter	Range
Frequency	25 MHz
Frequency Tolerance (at 25℃)	±30 ppm
Shunt Capacitance	7pF Max
Drive Level	59.12uW/MHz
Load Capacitance	27pF
Aging (at 25℃)	±3ppm / year Max

3.4.2.1 STM32F103CB_OSC

Parameter	Range
Frequency	8 MHz
Frequency Tolerance (at 25℃)	±25 ppm
Load Capacitance	C≤15pF
Aging (at 25℃)	±5ppm / year Max

3.4.3 SPI Timing

3.4.3.1 W5200_SPI

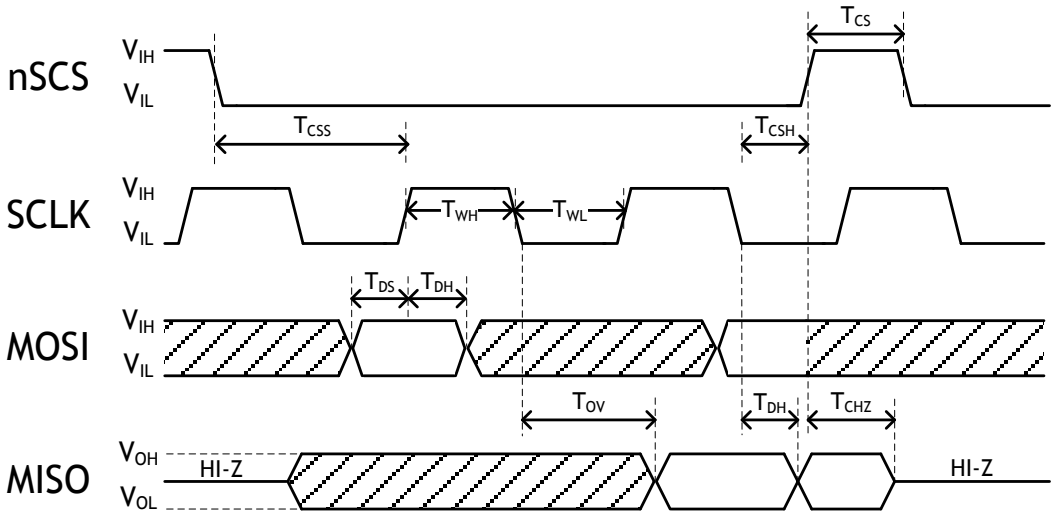


Figure 6 W5200_SPI Timing

Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		80	MHz
T_{WH}	SCK High Time	6		ns
T_{WL}	SCK Low Time	6		ns
T_{CS}	nSCS High Time	5		ns
T_{CSS}	nSCS Hold Time	5	-	ns
T_{CSH}	nSCS Hold Time	5		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{OV}	Output Valid Time		5	ns
T_{OH}	Output Hold Time	0		ns
T_{CHZ}	nSCS High to Output Hi-Z		5	ns

3.4.3.1 STM32F103CB_SPI

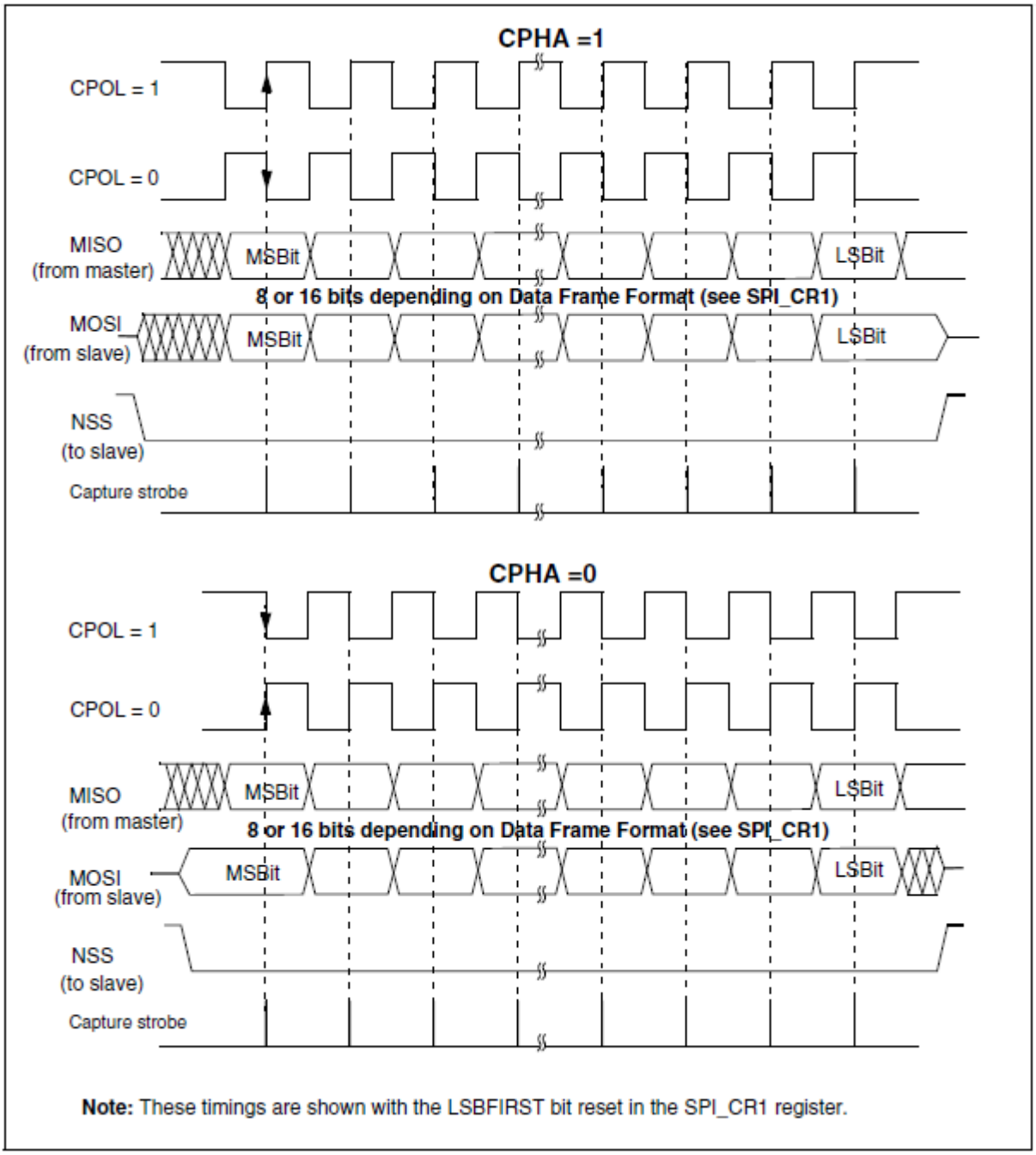


Figure 7 STM32F103CB_SPI Timing

3.4.4 Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1	1:1
Inductance	350 uH	350 uH

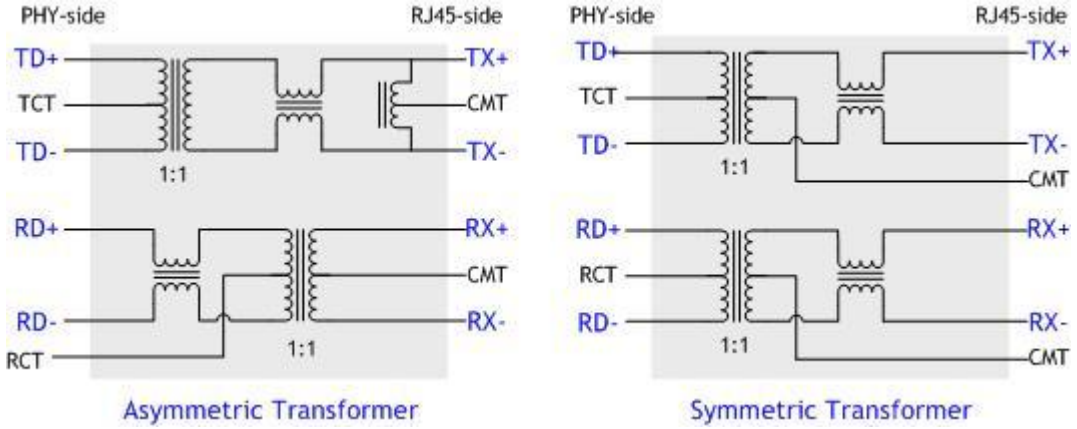


Figure 8 Transformer Type

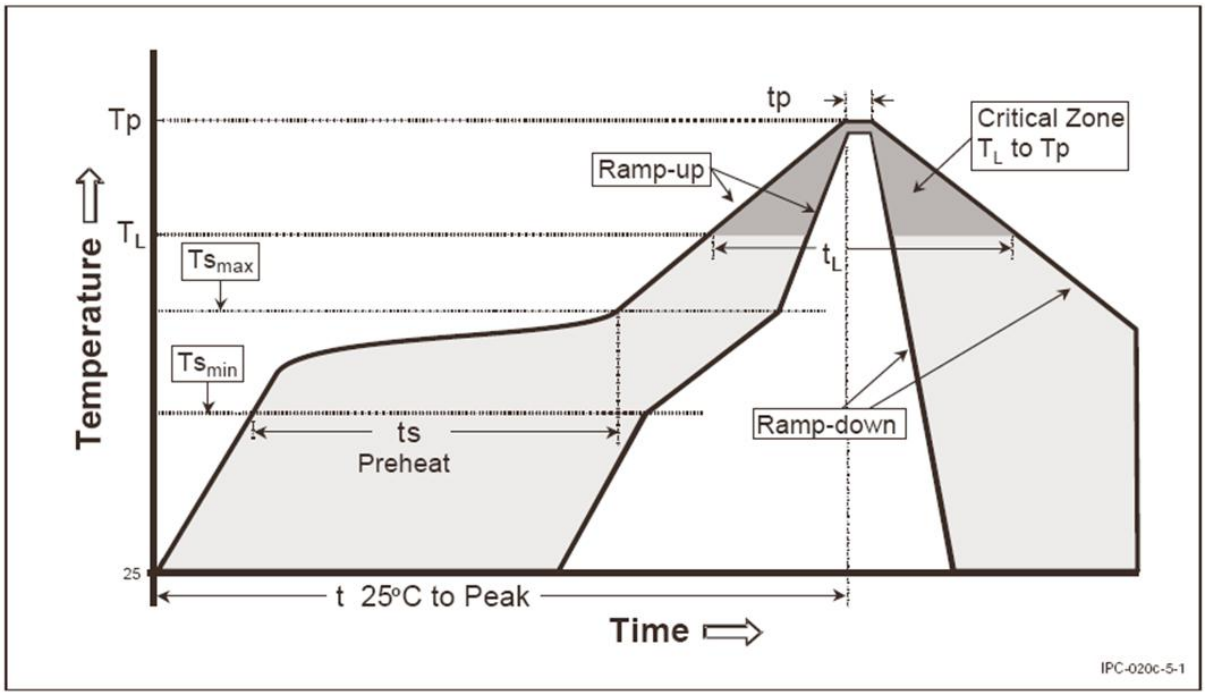
In case of using internal PHY mode, be sure to use symmetric transformer in order to support Auto MDI/MDIX(Crossover).

4 IR Reflow Temperature Profile (Lead-Free)

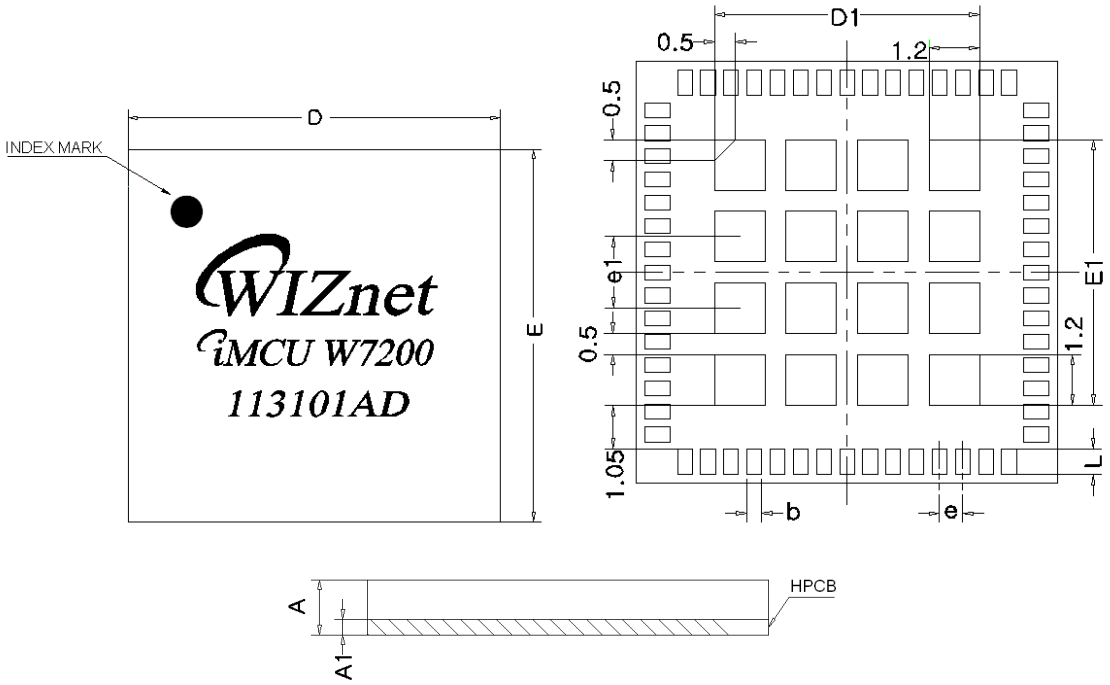
Moisture Sensitivity Level : 3

Dry Pack Required: Yes

Average Ramp-Up Rate (Ts_{max} to Tp)	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 150 °C 200 °C 60-120 seconds
Time maintained above: – Temperature (TL) – Time (tL)	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	265 + 0/-5°C
Time within 5 °C of actual Peak Temperature (tp)	30 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

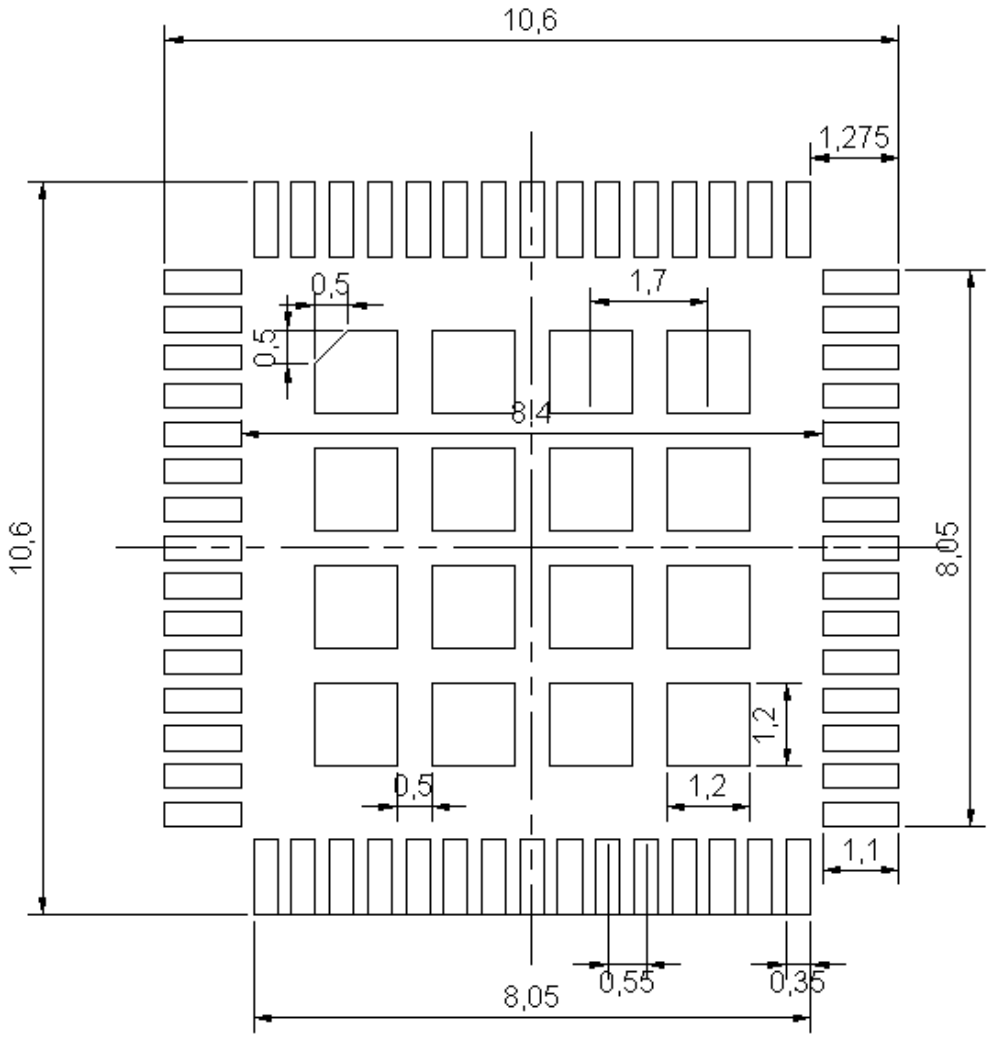


5 Package Descriptions



SIMBOL	Min	Normal	Max
A	1.3	1.4	1.5
A1	-	0.4	-
b	0.33	0.35	0.37
D		10.00 BSC	
D1	6.28	6.3	6.32
E		10.00 BSC	
E1	6.28	6.3	6.32
e	0.53	0.55	0.57
e1	1.68	1.7	1.72
L	0.58	0.6	0.62

6 Land Pattern Recommendation



Document History Information

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