WizFi630S
Hardware Design Guide

(Version 1.0.0)

For more information, please visit our website at http://www.wiznet.io/

Document Revision History

Date	Revision	Changes
2019-11-14	1.0	Release

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1. Introduction

This document has been prepared to better help the design-in process of WizFi630S.

Please utilize our forum and website for in depth technical support.

We greatly welcome and value your feedback and thank you for your interest in WizFi630S.

WIZnetForum

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2. Overview

Please use this guide as a reference since this document will suggest some hardware solutions with precautions but the suggested schematic and solutions will not be applied in every cases.

3. Pin Description

3.1 Pin map

The WizFi630S supports below pin-map based on default firmware.

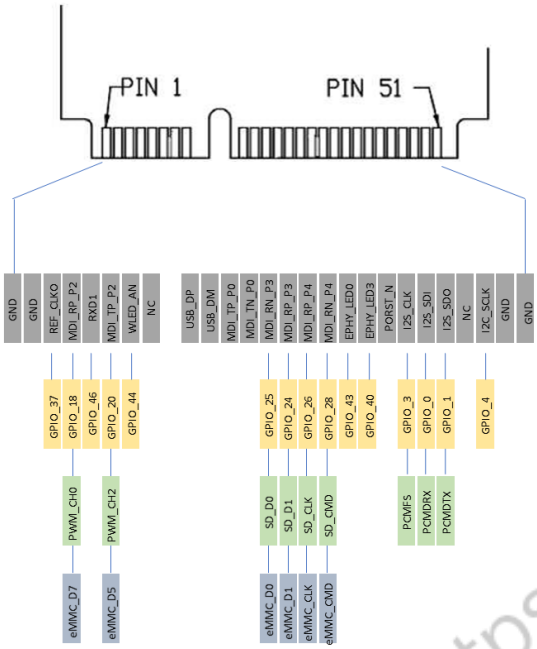
No	Type	Name	Shared	Description
1		GND		

2		3.3V		
3		GND		
4		3.3V		
5	I/O, IPD	REF_CLKO	GPIO#37	Will be provided as UART1 CTS-N
6	I/O, IPD	WDT_RST_N	GPIO#38	Will be provided as UART1 RTS-N
7	I/O, IPD	RXIP2	GPIO#18	Reserved
8	I/O, IPD	RXIM2	GPIO#19	Reserved
9	I/O, IPD	RxD1	GPIO#46	UART1 RXD
10	I/O, IPD	TxD1	GPIO#45	UART1 TXD
11	I/O, IPD	TXOP2	GPIO#20	Reserved
12	I/O, IPD	TXOM2	GPIO#21	Reserved
13	O	WLAN_LED	GPIO#44	Wireless Init On
14		NC		
15		NC(VBUS)		USB OTG VBUS pin in WizFi630
16		NC		
17	I/O	USB_PADP		USB OTG data pin Data+
18	I/O, IPD	UART_RX	GPIO#13	UART0 RxD
19	I/O	USB_PADM		USB OTG data pin Data-
20	I/O, IPD	UART_TX	GPIO#12	UART0 TxD
21	O	TXOP0		10/100 PHY Port #0 TXP
22	I	RXIM0		10/100 PHY Port #0 RXN
23	O	TXOM0		10/100 PHY Port #0 TXN
24	I	RXIP0		10/100 PHY Port #0 RXP
25	I	RXIM3	GPIO#25	10/100 PHY Port #3 RXN
26	O	TXOP3	GPIO#22	10/100 PHY Port #3 TXP
27	I	RXIP3	GPIO#24	10/100 PHY Port #3 RXP
28	O	TXOM3	GPIO#23	10/100 PHY Port #3 TXN
29	I	RXIP4	GPIO#26	10/100 PHY Port #4 RXP
30	O	TXOM4	GPIO#27	10/100 PHY Port #4 TXN
31	I	RXIM4	GPIO#28	10/100 PHY Port #4 RXN
32	O	TXOP4	GPIO#29	10/100 PHY Port #4 TXP
33	O	LINK0_LED	GPIO#43	LAN port 0 Link LED
34	O	LINK4_LED	GPIO#39	LAN port 4 Link LED
35	O	LINK3_LED	GPIO#40	LAN port 3 Link LED

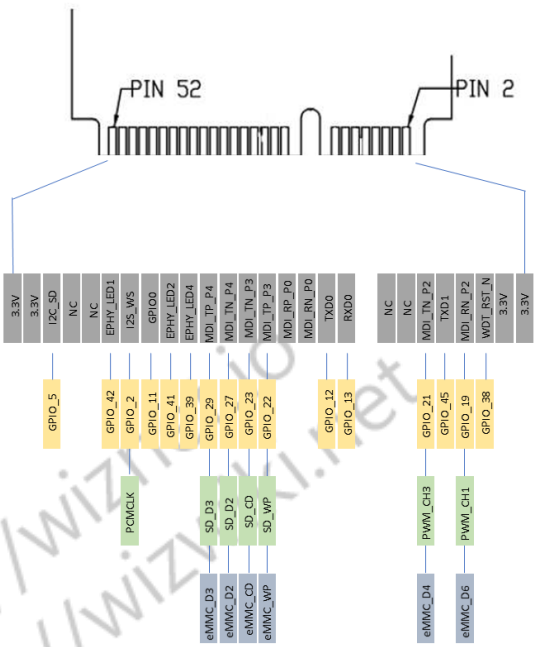
36	I/O, IPD	LINK2	GPIO#41	WPS Button Push
37	I, IPU	CPURST_N		
38	I/O, IPD	GPIO_0	GPIO#11	Reset Button Push
39	I/O, IPD	I2S_CLK	GPIO#3	General Purpose Output LED
40	I/O, IPD	I2S_WS	GPIO#2	General Purpose Input Switch SW1-1
41	I/O, IPD	I2S_SDI	GPIO#0	General Purpose Output LED
42	I/O, IPD	LINK1	GPIO#42	WPS LED
43		I2S_DO	GPIO#1	GPIO
44		NC		
45		NC		
46		NC		
47	I/O, IPD	I2C_SCLK	GPIO#4	General Purpose Input Switch SW1-2
48	I/O, IPD	I2C_SD	GPIO#5	RUN LED
49		GND		
50		3.3V		
51		GND		
52		3.3V		

3.3 Pin layout

mini PCIe connector Top View



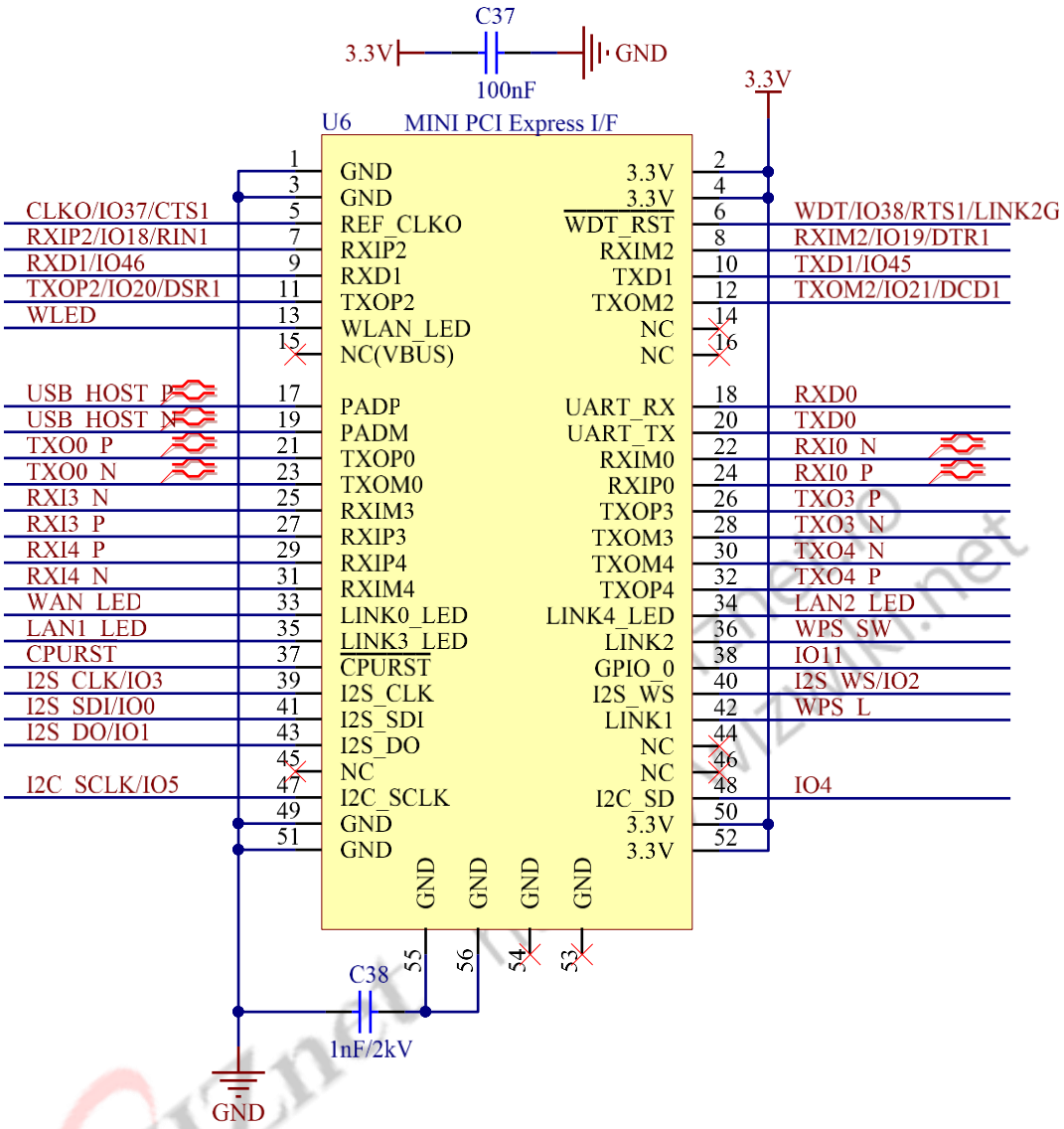
mini PCIe connector Bottom View



4. Recommended Circuit Diagram

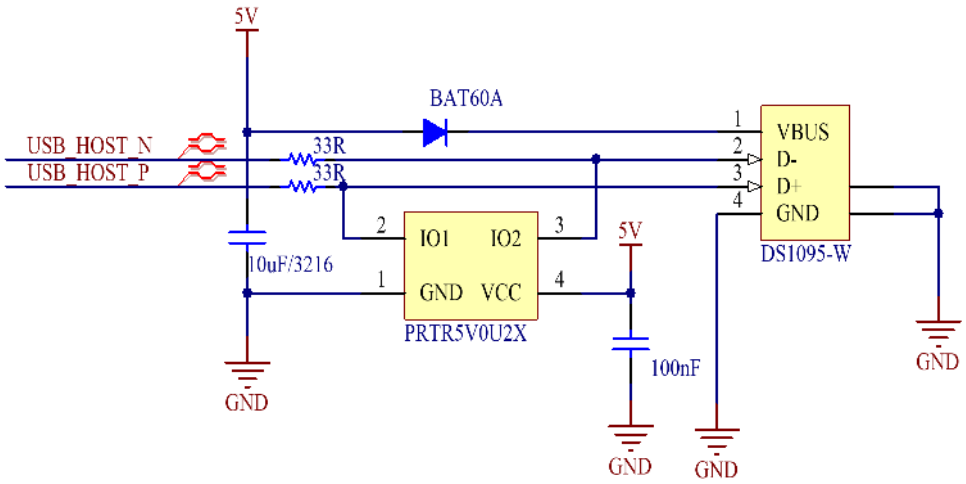
4.1 Basic schematic Design of the WizFi630S

When designing the schematic, the USB HOST line (PADP & PADM) should be paired with the Ethernet line P & M (ex: TXOP0, TXOM0). C37 must be close to the 3.3V and connecting C38 to the Mini PCI Express port will decrease noise.

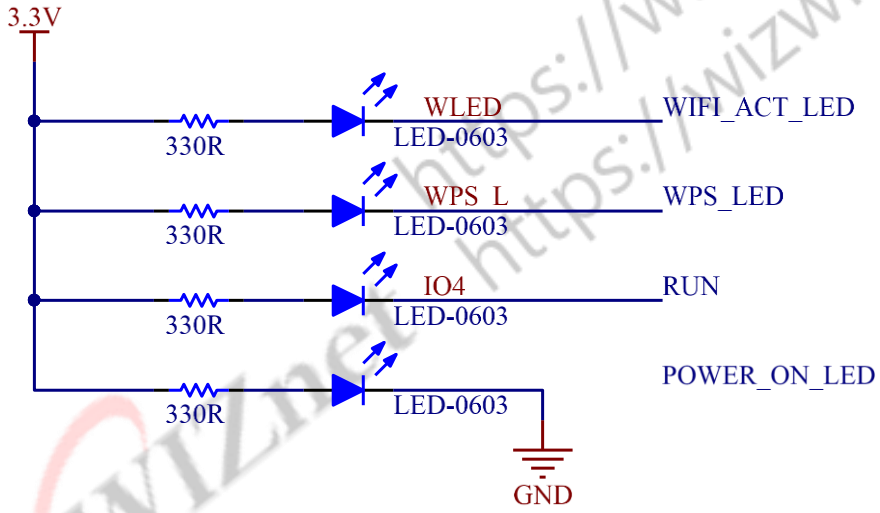


4.2 USB Host Schematic Design

We recommend pairing the USB HOST P and N line, and also place the diode as shown below for ESD protection



4.3 LED Schematic Design

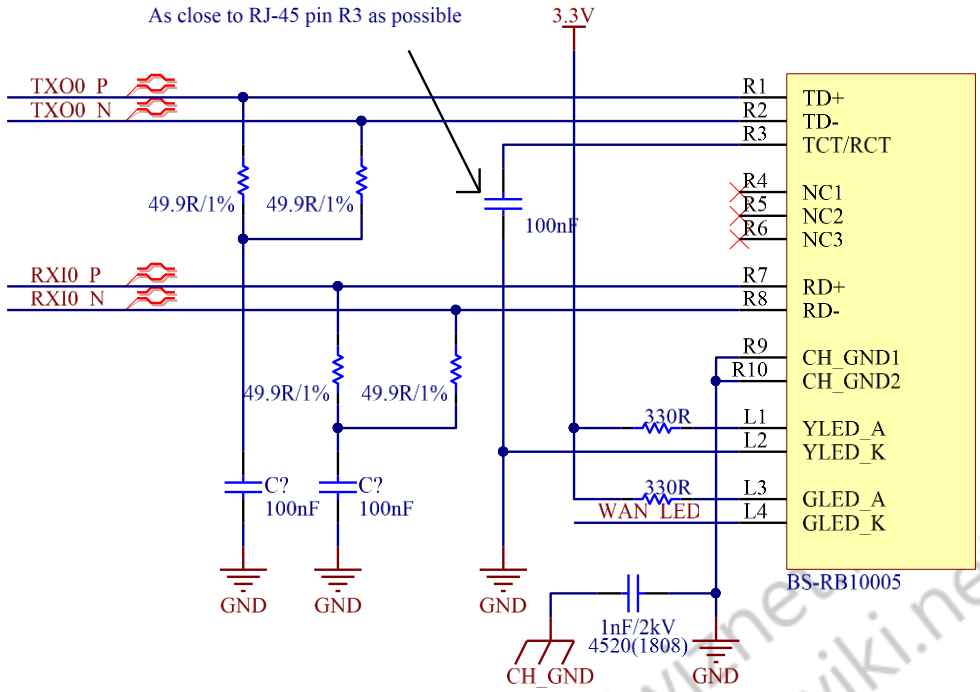


4.4 Ethernet Schematic Design

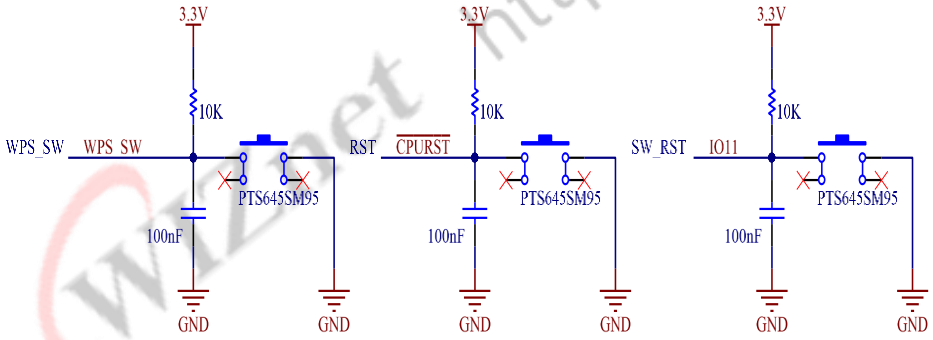
We also recommend paring the P and N line for Ethernet schematic, and do not place R, L, C, other sign lines below the RJ-45 schematic (especially not below the pair line).

The Center-Tap of WizFi630S connects to GND whereas the Center-Tap of WizFi630A operates in 1.8V ~ 3.3V.

Another recommendation is to isolate the CH_GND and GND with a 1nF/2kV capacity.

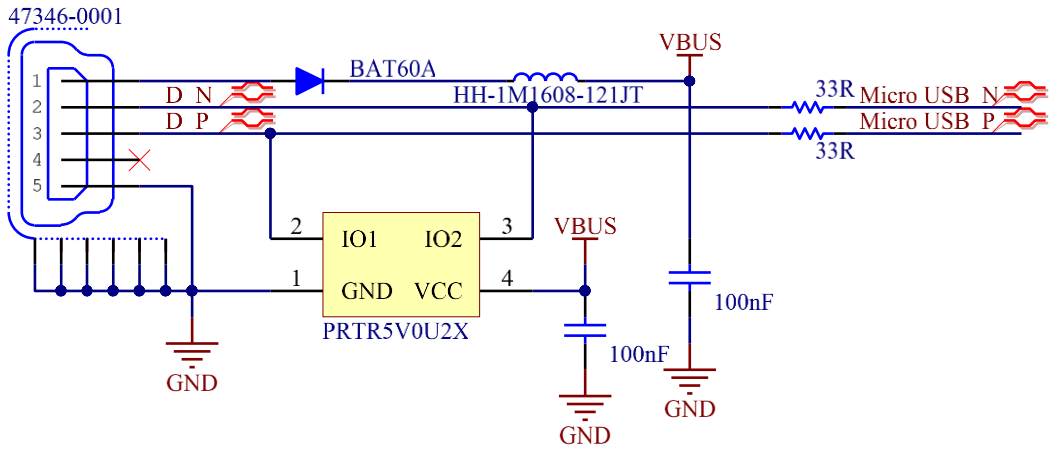


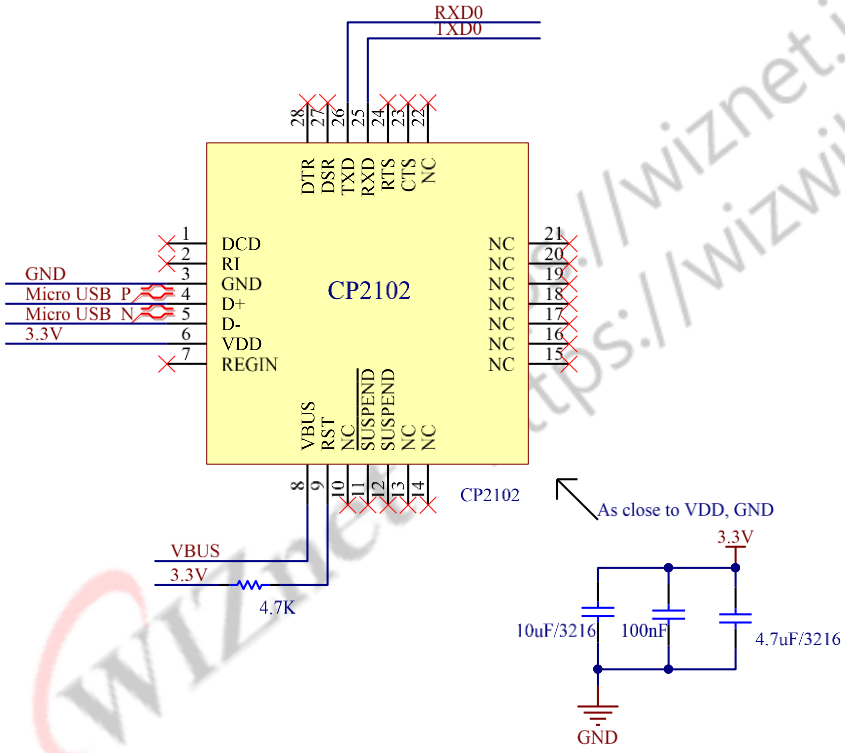
4.5 Switch Schematic Design



4.6 UART0 Micro USB Schematic Design

Micro USB P should be paired with N line, and we recommend placing the diode as shown below for ESD protection.





5. Power Supply

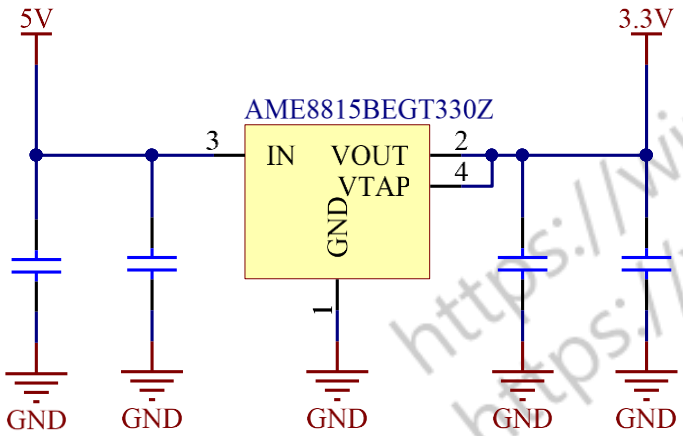
Power supply is one of the critical parts in the design stage that will affect the performance so please refer to the guidelines below.

5.1 Power Supply Requirements

Type	Description
Voltage Rating	DC 3.3V
Current Rating	1A

Caution

You must not exceed the voltage rating of DC 3.3V, otherwise WizFi630S will not operate as designed and could cause damage to the device. Also, please design with at least 1.5 or 2 times more current rating (1.5A) ~ (2A) for similar reasons specified ahead.



6. Power Supply

Refer to the Mini PCIe socket datasheet since WizFi630S uses a Mini PCIe connector.

6.1 Dimensions

Dimensions (mm)	Length	Width	Height	Hole Width	HOLE Height	HOLE Φ	PCB Thickness
	43	33	3.8	24.2	3	2.5	1.0
	Tolerance +/- 0.1mm