W55RP20 Datasheet

Version 1.0.2

http://www.wiznet.co.kr

Table of Contents

List of table

List of figures

1 Introduction

This chip is a System-in-Package (SiP) solution that integrates WIZnet's W5500 Ethernet controller with the RP2040 microcontroller from Raspberry Pi, providing networking and processing capabilities for IoT devices and smart applications. The W5500 supports a hardware TCP/IP stack, simplifying network connectivity and communication management, and offers an efficient solution without the need for external memory. The RP2040 features a dual-core ARM Cortex-M0+ processor, enabling fast data processing and multitasking capabilities to handle multiple tasks simultaneously.

This chip is designed to be compatible with various programming environments, supporting languages such as Python and C/C++, making it easier for developers to implement applications. Additionally, it supports various external interfaces and GPIO, ADC, UART, SPI, and I2C, facilitating connections with sensors, actuators, and other peripheral devices.

Key Features:

- Dual ARM Cortex-M0+ processor cores, up to 133MHz (or 200MHz at 1.15V)
- Hardwired TCP/IP stack
- 2MByte Flash memory on-chip
- 264kB on-chip SRAM in six independent banks
- DMA controller
- Fully-connected AHB crossbar
- Interpolator and integer divider peripherals
- On-chip programmable LDO to generate core voltage
- 2 on-chip PLLs to generate USB and core clocks
- 23 GPIO pins, 4 of which can be used as analogue inputs
- Peripherals
  - 2 UARTs
  - 2 SPI controllers
  - 2 I2C controllers
  - 16 PWM channels
  - USB 1.1 controller and PHY, with host and device support
  - 8 PIO state machines
- Supported Network Protocols
  - TCP
  - UDP
  - IPv4
  - ICMP
  - ARP
  - IGMP
  - PPPoE

2 Description

Figure 1. W55RP20 Chip

The main clock speed of the W55RP20 supports a CPU frequency of up to 133MHz (or 200MHz at 1.15V), and it has 2 MB of flash memory and 264 kB of SRAM built-in. It includes an integrated Ethernet PHY and is equipped with a total of 5 timers (1 Watchdog Timer and 4 General Timers).

Additionally, it supports up to 16 PWM channels and up to 2 UART, SPI, and I2C communication interfaces. There are a total of 8 TCP/IP sockets, 23 GPIO pins, and 12 DMA channels. The operating voltage range is from 1.8V to 3.3V, and the operating temperature range is from -40°C to 85°C.

For specific information about the chip, please refer to the [1]RP2040 Datasheet and [2]W5500 Datasheet.

The SDK supports various development environments such as C/C++, MicroPython, CircuitPython, FreeRTOS, Arduino, and LwIP, and it provides protocol supports such as AWS, Azure, TLS, SSL, MQTT, and HTTP.

Table 1. W55RP20 features and peripheral counts

Peripherals		W55RP20
Flash memory in Mbytes		2Mbytes
SRAM in Kbytes		264kB on-chip SRAM in six independent banks
Timer	Watch Dog	1
	Timer	4
	PWM	Up to 16
Comm	UART	Up to 2
	SPI	Up to 2
	TCP/IP Socket	8
Internal PHY		Yes
GPIOs		23-GPIO pins
DMA channel		12ch
CPU frequency		up to 133MHz (or 200MHz at 1.15V)
Operating voltage		1.8 to 3.3 DC
Operating temperatures		-40℃ to 85℃
Package		QFN68, 8x8mm

[1] RP2040 Datasheet Link : https://docs.wiznet.io/Product/ioNIC/W55RP20/documents_md#rp2040-datasheet
[2] W5500 Datasheet Link : https://docs.wiznet.io/Product/iEthernet/W5500/datasheet

3 Pinout and descriptions

3.1 Pin layout

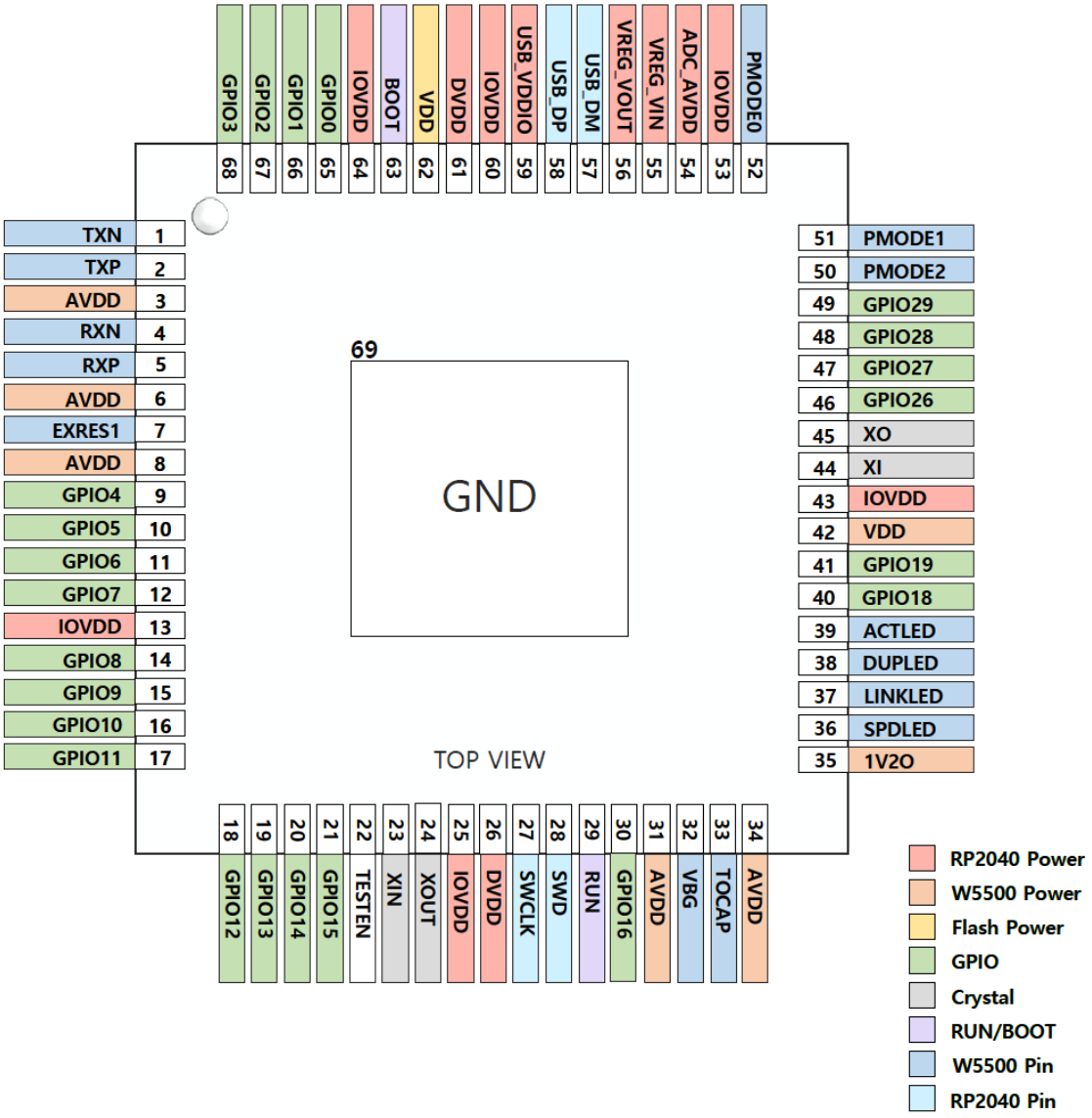

Figure 2. W55RP20 pin layout

3.2 Pin description

Table 2. Pin Type Notation

Type	Description
I	Input
O	Output
I/O	Input / Output
A	Analog
PWR	3.3V power
GND	Ground

Table 3. W55RP20 Pin Description

Pin No	Symbol	Chip	Type	Description
1	TXN	W5500	AO	**TXP/TXN differential signal pair** The differential data is transmitted to the media on the TXP/TXN signal pair.
2	TXP	W5500	AO	
3	AVDD	W5500	PWR	**TOE Analog 3.3V power**
4	RXN	W5500	AI	**RXP/RXN differential signal pair** The differential data from the media is received on the RXP/RXN signal pair
5	RXP	W5500	AI	
6	AVDD	W5500	PWR	**TOE Analog 3.3V power**
7	EXRES1	W5500	AI/O	**External Resistor pin** Connect a resistor of 12.4KΩ to the AGND. (Refer to the “Reference schematic”)
8	AVDD	W5500	PWR	**TOE Analog 3.3V power**
9	GPIO4	RP2040	I/O	General-purpose digital input and output.
10	GPIO5	RP2040	I/O	General-purpose digital input and output.
11	GPIO6	RP2040	I/O	General-purpose digital input and output.
12	GPIO7	RP2040	I/O	General-purpose digital input and output.
13	IOVDD	RP2040	PWR	**Digital IO Supply** Power supply for digital GPIOs, nominal voltage 3.3V
14	GPIO8	RP2040	I/O	General-purpose digital input and output.
15	GPIO9	RP2040	I/O	General-purpose digital input and output.
16	GPIO10	RP2040	I/O	General-purpose digital input and output.
17	GPIO11	RP2040	I/O	General-purpose digital input and output.
18	GPIO12	RP2040	I/O	General-purpose digital input and output.
19	GPIO13	RP2040	I/O	General-purpose digital input and output.
20	GPIO14	RP2040	I/O	General-purpose digital input and output.
21	GPIO15	RP2040	I/O	General-purpose digital input and output.
22	TESTEN	RP2040	I	**Factory test mode pin** Tie to GND.
23	XIN	RP2040	AI	**Crystal input/output** Connect a crystal to RP2040’s crystal oscillator. XIN can also be used as a single-ended CMOS clock input, with XOUT disconnected. The USB bootloader requires a 12MHz crystal or 12MHz clock input.
24	XOUT	RP2040	AO	
25	IOVDD	RP2040	PWR	**Digital IO Supply** Power supply for digital GPIOs, nominal voltage 3.3V
26	DVDD	RP2040	PWR	**Digital core power supply** nominal voltage 1.1V. Can be connected to VREG_VOUT, or to some other board-level power supply.
27	SWCLK	RP2040	O	**Debug clock/data** Access to the internal Serial Wire Debug multi-drop bus. Provides debug access to both
28	SWD	RP2040	I/O	

				processors, and can be used to download code.
29	RUN	RP2040	I	**Global asynchronous reset pin** Reset when driven low, run when driven high. If no external reset is required, this pin can be tied directly to IOVDD.
30	GPIO16	RP2040	I/O	General-purpose digital input and output.
31	AVDD	W5500	PWR	**TOE Analog 3.3V power**
32	VBG	W5500	AO	**Output of band gap**
33	TOCAP	W5500	AO	**External Reference Capacitor** This pin must be connected to a 4.7uF capacitor. The trace length to capacitor should be short to stabilize the internal signals.
34	AVDD	W5500	PWR	**TOE Analog 3.3V power**
35	1V2O	W5500	PWR	**1.2V regulator output voltage** Connect 10nF capacitor.
36	SPDLED	W5500	O	**Speed LED** This shows the Speed status of the connected link. Low: 100Mbps High: 10Mbps
37	LINKLED	W5500	O	**Link LED** This shows the Link status. Low: Link is established High: Link is not established
38	DUPLED	W5500	O	**Duplex LED** This shows the Duplex status for the connected link. Low: Full-duplex mode High: Half-duplex mode
39	ACTLED	W5500	O	**Active LED** This shows that there is Carrier sense (CRS) from the active Physical Medium Sub-layer (PMD) during TX or RX activity. Low: Carrier sense from the active PMD High: No carrier sense
40	GPIO18	RP2040	I/O	General-purpose digital input and output.
41	GPIO19	RP2040	I/O	General-purpose digital input and output.
42	VDD	W5500	PWR	**TOE Digital 3.3V Power**
43	IOVDD	RP2040	PWR	**Digital IO Supply** Power supply for digital GPIOs, nominal voltage 3.3V
44	XI	W5500	AI	**25MHz crystal input/output** A 25MHz crystal and oscillator is used to connect these pins.
45	XO	W5500	AO	
46	GPIO26/ADC0	RP2040	I/O	General-purpose digital input and output, with analogue-to-digital converter function.
47	GPIO27/ADC1	RP2040	I/O	General-purpose digital input and output, with analogue-to-digital converter function.
48	GPIO28/ADC2	RP2040	I/O	General-purpose digital input and output, with analogue-to-digital converter function.
49	GPIO29/ADC3	RP2040	I/O	General-purpose digital input and output, with

<table>
<tr><td></td><td></td><td></td><td></td><td>analogue-to-digital converter function.</td></tr>
<tr><td>50</td><td>PMODE2</td><td>W5500</td><td>I</td><td rowspan="3">PHY Operation mode select pins
These pins determine the network mode. Refer to the below table for details.
Default: Pull-up(77kΩ)
<table><tr><th colspan="3">PMODE[2:0]</th><th rowspan="2">Description</th></tr><tr><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>10BT Half-duplex,
Auto-negotiation disabled</td></tr><tr><td>0</td><td>0</td><td>1</td><td>10BT Full-duplex,
Auto-negotiation disabled</td></tr><tr><td>0</td><td>1</td><td>0</td><td>100BT Half-duplex,
Auto-negotiation disabled</td></tr><tr><td>0</td><td>1</td><td>1</td><td>100BT Full-duplex,
Auto-negotiation disabled</td></tr><tr><td>1</td><td>0</td><td>0</td><td>100BT Half-duplex,
Auto-negotiation enabled</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Not used</td></tr><tr><td>1</td><td>1</td><td>1</td><td>All capable,
Auto-negotiation enabled</td></tr></table></td></tr>
<tr><td>51</td><td>PMODE1</td><td>W5500</td><td>I</td></tr>
<tr><td>52</td><td>PMODE0</td><td>W5500</td><td>I</td></tr>
<tr><td>53</td><td>IOVDD</td><td>RP2040</td><td>PWR</td><td>Digital IO Supply
Power supply for digital GPIOs, nominal voltage 3.3V.</td></tr>
<tr><td>54</td><td>ADC_AVDD</td><td>RP2040</td><td>PWR</td><td>ADC supply
Power supply for analogue-to-digital converter, nominal voltage 3.3V.</td></tr>
<tr><td>55</td><td>VREG_VIN</td><td>RP2040</td><td>PWR</td><td>Voltage regulator input supply
Power input for the internal core voltage regulator, nominal voltage 1.8V to 3.3V.</td></tr>
<tr><td>56</td><td>VREG_VOUT</td><td>RP2040</td><td>PWR</td><td>Voltage regulator output
Power output for the internal core voltage regulator, nominal voltage 1.1V, 100mA max current.</td></tr>
<tr><td>57</td><td>USB_DM</td><td>RP2040</td><td>I/O</td><td rowspan="2">USB controller, supporting Full Speed device and Full/Low Speed host. A 27Ω series termination. resistor is required on each pin, but bus pullups and pulldowns are provided internally.</td></tr>
<tr><td>58</td><td>USB_DP</td><td>RP2040</td><td>I/O</td></tr>
<tr><td>59</td><td>USB_VDD</td><td>RP2040</td><td>PWR</td><td>USB supply
Power supply for internal USB Full Speed PHY, nominal voltage 3.3V</td></tr>
<tr><td>60</td><td>IOVDD</td><td>RP2040</td><td>PWR</td><td>Digital IO Supply</td></tr>
</table>

				Power supply for digital GPIOs, nominal voltage 3.3V
61	DVDD	RP2040	PWR	Digital core power supply, nominal voltage 1.1V. Can be connected to VREG_VOUT, or to some other board-level power supply
62	VDD	Flash	PWR	Power supply of the Flash Memory
63	BOOT	RP2040	I	**BOOT Pin** When power is applied and during reset, if the BOOT pin is low, the device enters BOOTSEL mode.
64	IOVDD	RP2040	PWR	**Digital IO Supply** Power supply for digital GPIOs, nominal voltage 3.3V
65	GPIO0	RP2040	I/O	General-purpose digital input and output.
66	GPIO1	RP2040	I/O	General-purpose digital input and output.
67	GPIO2	RP2040	I/O	General-purpose digital input and output.
68	GPIO3	RP2040	I/O	General-purpose digital input and output.
69	GND	Common	GND	Ground

4 Functional Overview

- External Memory Execution: Code can be executed directly from external memory via SPI, I2C, or QSPI interfaces.
- Debug Interface: Available through the SWD interface.
- Internal SRAM: Addressable 264 kB area, divided into 6 banks allowing parallel access.
- DMA Bus Master: Offloads repetitive data transfer tasks from the processor.
- GPIO Control: Can be driven directly or through various dedicated logic functions.
- PIO Controllers: Can provide a variety of IO functions.
- USB Controllers: Provides FS/LS host or device connectivity under software control via the integrated PHY.
- ADC: There are 4 ADC inputs shared with GPIO pins.
- PLLs: Two PLLs provide a fixed 48MHz clock for USB or ADC and a system clock up to 133MHz (or 200MHz at 1.15V).
- Internal Voltage Regulator: Supplies core voltage, so the final product only needs to supply IO voltage.

4.1 System Architecture

In the W55RP20, the W5500 Ethernet controller is internally connected to the RP2040 MCU through an internal SPI interface.

This SPI interface is not exposed to external pins and is reserved exclusively for internal communication between the RP2040 and the W5500.

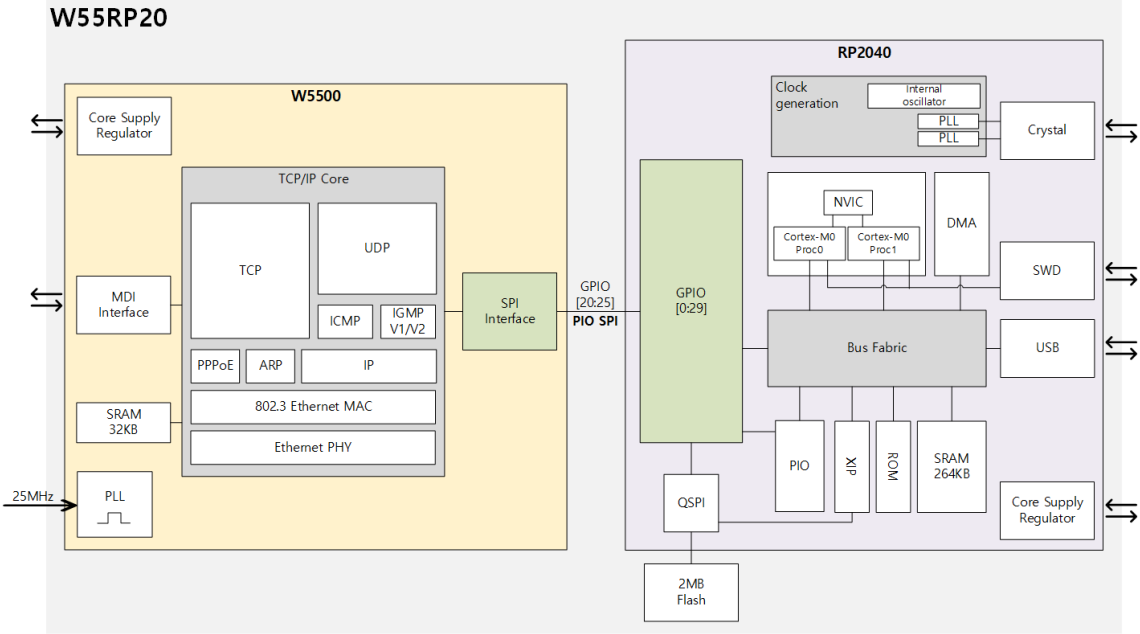

Figure 3. W55RP20 System Architecture

Table 4. Internal Connection between RP2040 and W5500

RP2040	W5500	Description
GPIO20	SPI_CS	Internal SPI chip select
GPIO21	SPI_SCK	Internal SPI clock
GPIO22	SPI_MISO	Internal SPI data output
GPIO23	SPI_MOSI	Internal SPI data input
GPIO24	INTn	Internal interrupt signal
GPIO25	RSTn	Internal reset control

4.2 Boot sequence

The boot sequence of the W55RP20 involves the coordinated operation of several components until the processor resets and the bootrom is executed. Before the processor begins execution, the bootrom is launched through the following sequence:

- Power is supplied to the chip, and the RUN pin goes high.
- The On-Chip Voltage Regulator waits until the digital core supply (DVDD) is stabilized.
- The Power-On State Machine starts, and the bootrom is executed.

4.2.1 Bootrom

The bootrom is a 16 KB embedded software within the chip, responsible for the "processor-controlled" phase of the boot sequence. It includes the following functionalities:

- Processor core0 initial boot sequence
- Processor core1 low power wait and launch protocol
- USB MSC class-compliant bootloader with UF2 support for downloading code/data to FLASH or RAM
- USB PICOBOOT bootloader interface for advanced management
- Routines for programming and manipulating the external flash
- Fast floating point library
- Fast bit counting / manipulation functions
- Fast memory fill/copy functions

For more detailed information, please refer to sections 2.7 Boot Sequence and 2.8 Bootrom in the RP2040 datasheet.

4.3 Memories

The W55RP20 includes 16 Kbytes of ROM, 264 Kbytes of SRAM, and 2 Mbytes of Flash.

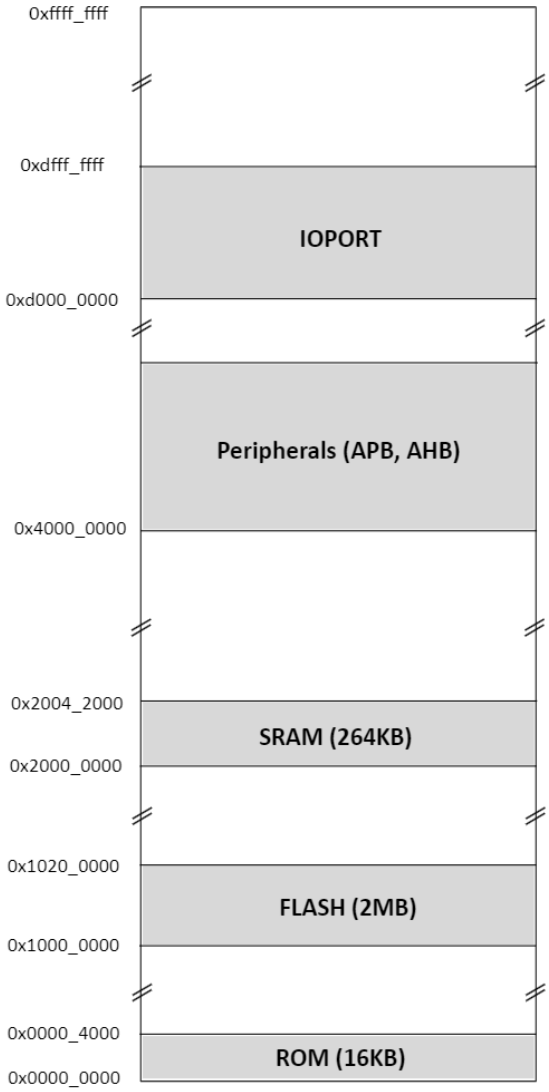

Figure 4. Memory Map

4.3.1 ROM

The ROM is located at address 0x0000_0000 and includes the following components:

- Initial startup routine
- Flash boot sequence
- Flash programming routines
- USB mass storage device with UF2 support
- Utility libraries such as fast floating point

4.3.2 SRAM

The SRAM is located at address 0x2000_0000 and is organized into four 64 KB banks and two 4 KB banks.

4.3.3 Flash

The Flash memory is located at address 0x1000_0000 and can be accessed via the QSPI interface through XIP.

- 100,000 Program / Erase Cycle
- 20-year Data Retention

Table 5. Flash Memory Organization

Block	Sector	Address range	
31	511	1FF000H	1FFFFFH
	...	...	...
	496	1F0000H	1F0FFFH
30	495	1EF000H	1EFFFFH
	...	...	...
	480	1E0000H	1E0FFFH
...	...	...	...
	...	...	...
	...	...	...
...	...	...	...
	...	...	...
	...	...	...
2	47	02F000H	02FFFFH
	...	...	...
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	...	...	...
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	...	...	...
	0	000000H	000FFFH

The Flash Access Function is as follows. For detailed examples using this function, please refer to the [3]RP2040 Flash example.

```
void flash_range_erase(uint32_t flash_offs, size_t count);

void flash_range_program(uint32_t flash_offs, const uint8_t *data, size_t count);
```

For more detailed information, please refer to sections 2.2 Address Map and 2.6 Memory in the RP2040 datasheet.

4.4 DMA

The W55RP20's Direct Memory Access (DMA) controller handles large data transfers, allowing the processor to switch to other tasks or low-power states. It supports memory-to-peripheral, peripheral-to-memory, and memory-to-memory transfers through 12 independent channels. Each channel has control and status registers for programming and monitoring. The DMA can read and write up to 32 bits of data per clock cycle, improving data throughput.

For more detailed information, please refer to section 2.5 DMA in the RP2040 datasheet.

[3] RP2040 Flash example Link: https://github.com/raspberrypi/pico-examples/blob/master/flash/program/flash_program.c

4.5 Power and Reset

4.5.1 Power Supplies

In most applications, some of these supplies can be combined and connected to a single power source. IOVDD, USB_VDD, and ADC_AVDD can be powered directly from a single 3.3V supply. DVDD is regulated from the 3.3V supply using the on-chip voltage regulator. VREG_OUT should be connected to the DVDD pin.

Detailed power supply parameters are provided in Section 5.4.5, “Power Supplies”.

For more detailed information, please refer to section 2.9 Power Supplies and 5.6 Power Supplies in the RP2040 datasheet.

4.5.2 Power Control

The following methods can be used to reduce dynamic power in the W55RP20:

- Top-level clock gating of individual peripherals and functional blocks
- Automatic control of top-level clock gates based on processor sleep state
- On-the-fly changes to system clock frequency or system clock source
- Zero-dynamic-power DORMANT state, waking on GPIO event or RTC IRQ

The following methods can be used to reduce static power in the W55RP20:

- Place memories into state-retaining power down state
- Power gating on peripherals that support this, e.g. ADC, temperature sensor

For more detailed information, please refer to section 2.11 Power Control in the RP2040 datasheet.

4.5.3 Resets

The W55RP20's chip-level reset subsystem resets the entire chip to its initial state. This occurs under the following conditions:

- Initial power on
- During a power supply brown-out event
- Chip’s RUN pin is taken low
- via Rescue Debug port

This subsystem has two reset outputs: rst_n_psm and rst_n_dp. The rst_n_psm resets the entire chip except for the debug port, while rst_n_dp only resets the Rescue DP. Both outputs remain low during initial power on, brown-out events, and when the RUN pin is low. Additionally, rst_n_psm can be held low through the Rescue DP.

For more detailed information, please refer to section 2.12 Chip-Level Reset in the RP2040 datasheet.

4.6 Clocks

4.6.1 Clocks

The clocks block of the W55RP20 provides independent clocks to internal and external components of the chip. It can receive multiple clock sources and allows clocks to be started or stopped independently.

Clock sources include an on-chip ring oscillator, a crystal oscillator, external clocks, and PLLs. The clock generator feature allows the selected clock source to be divided and output accordingly.

For more detailed information, please refer to section 2.15 Clocks in the RP2040 datasheet.

4.6.2 Crystal Oscillator (XOSC)

The XOSC in the W55RP20 uses an external crystal to generate an accurate reference clock. The W55RP20 supports crystals ranging from 1 MHz to 15 MHz.

For more detailed information, please refer to section 2.16 Crystal Oscillator (XOSC) in the RP2040 datasheet.

4.6.3 Ring Oscillator (ROSC)

The ROSC is an on-chip oscillator made up of a ring of inverters. It requires no external components and automatically starts when power is supplied.

For more detailed information, please refer to section 2.17 Ring Oscillator (ROSC) in the RP2040 datasheet.

4.6.4 PLL

The PLL (Phase-Locked Loop) is designed to take a reference clock and amplify the frequency using a Voltage Controlled Oscillator (VCO). Since the VCO must operate at high frequencies (750~1600 MHz), there are two dividers, pll_sys and pll_usb, that divide the VCO frequency before distributing it to the clock generator.

For more detailed information, please refer to section 2.18 PLL in the RP2040 datasheet.

4.7 GPIO

The W55RP20 has 30 multifunctional General Purpose Input/Output (GPIO) pins divided into two banks. Six pins from the QSPI bank are used for executing code from flash memory. The available pins are listed in the table below. GPIO26, GPIO27, GPIO28, and GPIO29 can also be used as inputs for the analog-to-digital converter.

Table 6. General Purpose Input/Output (GPIO) User Bank Functions

GPIO	F1	F2	F3	F4	F5	F6	F7	F9
0	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PIO0	PIO1	USB OVCUR DET
1	SPI0 CSn	UART0 RX	I2C0 SCL	PWM0 B	SIO	PIO0	PIO1	USB VBUS DET
2	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PIO0	PIO1	USB VBUS EN
3	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PIO0	PIO1	USB OVCUR DET
4	SPI0 RX	UART1 TX	I2C0 SDA	PWM2 A	SIO	PIO0	PIO1	USB VBUS DET
5	SPI0 CSn	UART1 RX	I2C0 SCL	PWM2 B	SIO	PIO0	PIO1	USB VBUS EN
6	SPI0 SCK	UART1 CTS	I2C1 SDA	PWM3 A	SIO	PIO0	PIO1	USB OVCUR DET
7	SPI0 TX	UART1 RTS	I2C1 SCL	PWM3 B	SIO	PIO0	PIO1	USB VBUS DET
8	SPI1 RX	UART1 TX	I2C0 SDA	PWM4 A	SIO	PIO0	PIO1	USB VBUS EN
9	SPI1 CSn	UART1 RX	I2C0 SCL	PWM4 B	SIO	PIO0	PIO1	USB OVCUR DET
10	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PIO0	PIO1	USB VBUS DET
11	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PIO0	PIO1	USB VBUS EN
12	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PIO0	PIO1	USB OVCUR DET
13	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PIO0	PIO1	USB VBUS DET
14	SPI1 SCK	UART0 CTS	I2C1 SDA	PWM7 A	SIO	PIO0	PIO1	USB VBUS EN
15	SPI1 TX	UART0 RTS	I2C1 SCL	PWM7 B	SIO	PIO0	PIO1	USB OVCUR DET
16	SPI0 RX	UART0 TX	I2C0 SDA	PWM0 A	SIO	PIO0	PIO1	USB VBUS DET
18	SPI0 SCK	UART0 CTS	I2C1 SDA	PWM1 A	SIO	PIO0	PIO1	USB OVCUR DET
19	SPI0 TX	UART0 RTS	I2C1 SCL	PWM1 B	SIO	PIO0	PIO1	USB VBUS DET
20 - 25	Reserved (Internal W5500 SPI)							
26	SPI1 SCK	UART1 CTS	I2C1 SDA	PWM5 A	SIO	PIO0	PIO1	USB VBUS EN
27	SPI1 TX	UART1 RTS	I2C1 SCL	PWM5 B	SIO	PIO0	PIO1	USB OVCUR DET
28	SPI1 RX	UART0 TX	I2C0 SDA	PWM6 A	SIO	PIO0	PIO1	USB VBUS DET
29	SPI1 CSn	UART0 RX	I2C0 SCL	PWM6 B	SIO	PIO0	PIO1	USB VBUS EN

For more detailed information, please refer to section 2.19 GPIO in the RP2040 datasheet.

4.8 PIO

The W55RP20 contains two identical PIO (Programmable Input/Output) blocks, one of which is used for communication with the W5500. PIO is a versatile hardware interface that can support various IO standards, including:

- 8080 and 6800 parallel bus
- I2C
- 3-pin I2S
- SDIO
- SPI, DSPI, QSPI
- UART
- DVI or VGA

For more detailed information, please refer to section 3. PIO in the RP2040 datasheet.

4.9 Peripheral

4.9.1 USB

The W55RP20 includes a USB 2.0 controller capable of operating at full speed (12 Mbps). When acting as a host, it can communicate with both low-speed (1.5 Mbps) and full-speed devices.

The USB controller hardware handles low-level USB protocol processing. Therefore, programmers need to configure the controller and manage data buffers according to the events occurring on the bus.

The USB registers start at a base address of 0x50110000 (defined as USBCTRL_REGS_BASE in SDK).

Table 7. List of USB registers

Offset	Name	Info
0x00	ADDR_ENDP	Device address and endpoint control
0x04	ADDR_ENDP1	Interrupt endpoint 1. Only valid for HOST mode.
0x08	ADDR_ENDP2	Interrupt endpoint 2. Only valid for HOST mode.
…	…	…
0x38	ADDR_ENDP14	Interrupt endpoint 14. Only valid for HOST mode.
0x3c	ADDR_ENDP15	Interrupt endpoint 15. Only valid for HOST mode.
0x40	MAIN_CTRL	Main control register
0x44	SOF_WR	Set the SOF (Start of Frame) frame number in the host controller
0x48	SOF_RD	Read the last SOF (Start of Frame) frame number seen
0x4c	SIE_CTRL	SIE control register
0x50	SIE_STATUS	SIE status register
0x54	INT_EP_CTRL	interrupt endpoint control register
0x58	BUFF_STATUS	Buffer status register
0x5c	BUFF_CPU_SHOULD_HANDLE	Which of the double buffers should be handled. Only valid if using an interrupt per buffer (i.e. not per 2 buffers).
0x60	EP_ABORT	Device only: Can be set to ignore the buffer control register for this endpoint in case you would like to revoke a buffer.
0x64	EP_ABORT_DONE	Device only: Used in conjunction with EP_ABORT.
0x68	EP_STALL_ARM	Device: this bit must be set in conjunction with the STALL bit in the buffer control register to send a STALL on EP0.
0x6c	NAK_POLL	Used by the host controller. Sets the wait time in microseconds before trying again if the device replies with a NAK.
0x70	EP_STATUS_STALL_NAK	Device: bits are set when the IRQ_ON_NAK or IRQ_ON_STALL bits are set.

0x74	USB_MUXING	Where to connect the USB controller. Should be to_phy by default.
0x78	USB_PWR	Overrides for the power signals in the event that the VBUS signals are not hooked up to GPIO.
0x7c	USBPHY_DIRECT	This register allows for direct control of the USB phy.
0x80	USBPHY_DIRECT_OVERRIDE	Override enable for each control in usbphy_direct
0x84	USBPHY_TRIM	Used to adjust trim values of USB phy pull down resistors.
0x8c	INTR	Raw Interrupts
0x90	INTE	Interrupt Enable
0x94	INTF	Interrupt Force
0x98	INTS	Interrupt status after masking & forcing

For more detailed information, please refer to section 4.1 USB in the RP2040 datasheet.

4.9.2 UART

The W55RP20 has two UART peripheral instances, supporting the following features:

- Separate 32 x 8 Tx FIFOs and 32 x 12 Rx FIFOs
- Programmable baud rate generator (up to 7.8 Mbaud)
- Addition and removal of standard asynchronous communication bits (start, stop, parity)
- Line break detection
- Programmable serial interface (5, 6, 7, 8 bits)
- 1 or 2 stop bits
- Programmable hardware flow control

The UART0 and UART1 registers start at base addresses of 0x40034000 and 0x40038000 respectively (defined as UART0_BASE and UART1_BASE in SDK).

Table 8. List of UART registers

Offset	Name	Info
0x000	UARTDR	Data Register, UARTDR
0x004	UARTRSR	Receive Status Register/Error Clear Register, UARTRSR/UARTECR
0x018	UARTFR	Flag Register, UARTFR
0x020	UARTILPR	IrDA Low-Power Counter Register, UARTILPR
0x024	UARTIBRD	Integer Baud Rate Register, UARTIBRD
0x028	UARTFBRD	Fractional Baud Rate Register, UARTFBRD
0x02c	UARTLCR_H	Line Control Register, UARTLCR_H
0x030	UARTCR	Control Register, UARTCR
0x034	UARTIFLS	Interrupt FIFO Level Select Register, UARTIFLS
0x038	UARTIMSC	Interrupt Mask Set/Clear Register, UARTIMSC
0x03c	UARTRIS	Raw Interrupt Status Register, UARTRIS
0x040	UARTMIS	Masked Interrupt Status Register, UARTMIS
0x044	UARTICR	Interrupt Clear Register, UARTICR
0x048	UARTDMACR	DMA Control Register, UARTDMACR
0xfe0	UARTPERIPHID0	UARTPeriphID0 Register

0xfe4	UARTPERIPHID1	UARTPeriphID1 Register
0xfe8	UARTPERIPHID2	UARTPeriphID2 Register
0xfec	UARTPERIPHID3	UARTPeriphID3 Register
0xff0	UARTPCELLID0	UARTPCellID0 Register
0xff4	UARTPCELLID1	UARTPCellID1 Register
0xff8	UARTPCELLID2	UARTPCellID2 Register
0xffc	UARTPCELLID3	UARTPCellID3 Register

For more detailed information, please refer to section 4.2 UART in the RP2040 datasheet.

4.9.3 I2C

The two identical I2C controllers in the W55RP20 are based on the Synopsys DW_app_i2c (v2.0.1) IP configuration and support the following features:

- Master or slave mode (default master)
- Standard mode, Fast mode, and Fast Plus mode
- Default slave address 0x055
- 10-bit address support in master mode
- 16-element transmit buffer
- 16-element receive buffer
- DMA capable
- Interrupt generation

The I2C0 and I2C1 registers start at base addresses of 0x40044000 and 0x40048000 respectively (defined as I2C0_BASE and I2C1_BASE in SDK).

Table 9. List of I2C registers

Offset	Name	Info
0x00	IC_CON	I2C Control Register
0x04	IC_TAR	I2C Target Address Register
0x08	IC_SAR	I2C Slave Address Register
0x10	IC_DATA_CMD	I2C Rx/Tx Data Buffer and Command Register
0x14	IC_SS_SCL_HCNT	Standard Speed I2C Clock SCL High Count Register
0x18	IC_SS_SCL_LCNT	Standard Speed I2C Clock SCL Low Count Register
0x1c	IC_FS_SCL_HCNT	Fast Mode or Fast Mode Plus I2C Clock SCL High Count Register
0x20	IC_FS_SCL_LCNT	Fast Mode or Fast Mode Plus I2C Clock SCL Low Count Register
0x2c	IC_INTR_STAT	I2C Interrupt Status Register
0x30	IC_INTR_MASK	I2C Interrupt Mask Register
0x34	IC_RAW_INTR_STAT	I2C Raw Interrupt Status Register
0x38	IC_RX_TL	I2C Receive FIFO Threshold Register
0x3c	IC_TX_TL	I2C Transmit FIFO Threshold Register
0x40	IC_CLR_INTR	Clear Combined and Individual Interrupt Register
0x44	IC_CLR_RX_UNDER	Clear RX_UNDER Interrupt Register
0x48	IC_CLR_RX_OVER	Clear RX_OVER Interrupt Register
0x4c	IC_CLR_TX_OVER	Clear TX_OVER Interrupt Register
0x50	IC_CLR_RD_REQ	Clear RD_REQ Interrupt Register
0x54	IC_CLR_TX_ABRT	Clear TX_ABRT Interrupt Register
0x58	IC_CLR_RX_DONE	Clear RX_DONE Interrupt Register

0x5c	IC_CLR_ACTIVITY	Clear ACTIVITY Interrupt Register
0x60	IC_CLR_STOP_DET	Clear STOP_DET Interrupt Register
0x64	IC_CLR_START_DET	Clear START_DET Interrupt Register
0x68	IC_CLR_GEN_CALL	Clear GEN_CALL Interrupt Register
0x6c	IC_ENABLE	I2C ENABLE Register
0x70	IC_STATUS	I2C STATUS Register
0x74	IC_TXFLR	I2C Transmit FIFO Level Register
0x78	IC_RXFLR	I2C Receive FIFO Level Register
0x7c	IC_SDA_HOLD	I2C SDA Hold Time Length Register
0x80	IC_TX_ABRT_SOURCE	I2C Transmit Abort Source Register
0x84	IC_SLV_DATA_NACK_ONLY	Generate Slave Data NACK Register
0x88	IC_DMA_CR	DMA Control Register
0x8c	IC_DMA_TDLR	DMA Transmit Data Level Register
0x90	IC_DMA_RDLR	DMA Transmit Data Level Register
0x94	IC_SDA_SETUP	I2C SDA Setup Register
0x98	IC_ACK_GENERAL_CALL	I2C ACK General Call Register
0x9c	IC_ENABLE_STATUS	I2C Enable Status Register
0xa0	IC_FS_SPKLEN	I2C SS, FS or FM+ spike suppression limit
0xa8	IC_CLR_RESTART_DET	Clear RESTART_DET Interrupt Register
0xf4	IC_COMP_PARAM_1	Component Parameter Register 1
0xf8	IC_COMP_VERSION	I2C Component Version Register
0xfc	IC_COMP_TYPE	I2C Component Type Register

For more detailed information, please refer to section 4.3 I2C in the RP2040 datasheet.

4.9.4 SPI

The two identical SPI controllers in the W55RP20 are based on the ARM Primecell Synchronous Serial Port (SSP) (PL022) and support the following features:

- Master or slave mode
- 8-depth Tx and Rx FIFOs
- Interrupt generation for providing FIFO data or indicating error conditions
- DMA capable
- Programmable clock speed
- Programmable data size (4~16 bits)

The SPI0 and SPI1 registers start at base addresses of 0x4003c000 and 0x40040000 respectively (defined as SPI0_BASE and SPI1_BASE in SDK).

Table 10. List of I2C registers

Offset	Name	Info
0x000	SSPCR0	Control register 0
0x004	SSPCR1	Control register 1
0x008	SSPDR	Data register
0x00c	SSPSR	Status register
0x010	SSPCPSR	Clock prescale register
0x014	SSPIMSC	Raw Interrupt mask set or clear register
0x018	SSPRIS	Raw interrupt status register
0x01c	SSPMIS	Masked interrupt status register
0x020	SSPICR	Interrupt clear register
0x024	SSPDMACR	DMA control register

0xfe0	SSPPERIPHID0	Peripheral identification registers
0xfe4	SSPPERIPHID1	Peripheral identification registers
0xfe8	SSPPERIPHID2	Peripheral identification registers
0xfec	SSPPERIPHID3	Peripheral identification registers
0xff0	SSPPCELLID0	PrimeCell identification registers
0xff4	SSPPCELLID1	PrimeCell identification registers
0xff8	SSPPCELLID2	PrimeCell identification registers
0xffc	SSPPCELLID3	PrimeCell identification registers

For more detailed information, please refer to section 4.4 SPI in the RP2040 datasheet.

4.9.5 PWM

The PWM block of the W55RP20 consists of 8 identical slices. Each slice can produce two PWM outputs or measure the frequency or duty cycle of an input signal. Up to 16 PWM outputs can be controlled, and all GPIO pins can be driven by the PWM block.

The PWM slices support the following features:

- 16-bit counter
- 8.4 fractional clock divider
- Two output channels with independent duty cycles ranging from 0% to 100%
- Dual-slope and trailing-edge modulation
- Edge detection input mode for frequency measurement
- Level detection input mode for duty cycle measurement
- Configurable counter wrap
- Interrupts and DMA requests on counter wrap

The PWM registers start at a base address of 0x40050000 (defined as PWM_BASE in SDK).

Table 11. List of PWM registers

Offset	Name	Info
0x00	CH0_CSR	Control and status register
0x04	CH0_DIV	INT and FRAC form a fixed-point fractional number.
0x08	CH0_CTR	Direct access to the PWM counter
0x0c	CH0_CC	Counter compare values
0x10	CH0_TOP	Counter wrap value
0x14	CH1_CSR	Control and status register
0x18	CH1_DIV	INT and FRAC form a fixed-point fractional number.
0x1c	CH1_CTR	Direct access to the PWM counter
0x20	CH1_CC	Counter compare values
0x24	CH1_TOP	Counter wrap value
…	…	…
0x8c	CH7_CSR	Control and status register
0x90	CH7_DIV	INT and FRAC form a fixed-point fractional number.
0x94	CH7_CTR	Direct access to the PWM counter

0x98	CH7_CC	Counter compare values
0x9c	CH7_TOP	Counter wrap value
0xa0	EN	This register aliases the CSR_EN bits for all channels.
0xa4	INTR	Raw Interrupts
0xa8	INTE	Interrupt Enable
0xac	INTF	Interrupt Force
0xb0	INTS	Interrupt status after masking & forcing

For more detailed information, please refer to section 4.5 PWM in the RP2040 datasheet.

4.9.6 Timer

The system timer peripheral in the W55RP20 provides a global microsecond timebase for the device and generates interrupts based on this timebase. The timer supports the following features:

- 64-bit single counter that increments once per microsecond
- Can be read via latching registers, allowing reading on a 32-bit bus without race conditions
- Four alarms

The Timer registers start at a base address of 0x40054000 (defined as TIMER_BASE in SDK).

Table 12. List of TIMER registers

Offset	Name	Info
0x00	TIMEHW	Write to bits 63:32 of time
0x04	TIMELW	Write to bits 31:0 of time
0x08	TIMEHR	Read from bits 63:32 of time
0x0c	TIMELR	Read from bits 31:0 of time
0x10	ALARM0	Arm alarm 0, and configure the time it will fire.
0x14	ALARM1	Arm alarm 1, and configure the time it will fire.
0x18	ALARM2	Arm alarm 2, and configure the time it will fire.
0x1c	ALARM3	Arm alarm 3, and configure the time it will fire.
0x20	ARMED	Indicates the armed/disarmed status of each alarm.
0x24	TIMERAWH	Raw read from bits 63:32 of time (no side effects)
0x28	TIMERAWL	Raw read from bits 31:0 of time (no side effects)
0x2c	DBGPAUSE	Set bits high to enable pause when the corresponding debug ports are active
0x30	PAUSE	Set high to pause the timer
0x34	INTR	Raw Interrupts
0x38	INTE	Interrupt Enable
0x3c	INTF	Interrupt Force
0x40	INTS	Interrupt status after masking & forcing

For more detailed information, please refer to section 4.6 Timer in the RP2040 datasheet.

4.9.7 Watchdog

The watchdog is a countdown timer that can reboot the chip when it reaches zero. It is useful for restarting the processor if software gets stuck in an infinite loop. The programmer must periodically write to the watchdog to prevent it from reaching zero.

The watchdog registers start at a base address of 0x40058000 (defined as WATCHDOG_BASE in SDK).

Table 13. List of WATCHDOG registers

Offset	Name	Info
0x00	CTRL	Watchdog control
0x04	LOAD	Load the watchdog timer.
0x08	REASON	Logs the reason for the last reset.
0x0c	SCRATCH0	Scratch register
0x10	SCRATCH1	Scratch register
…	…	…
0x28	SCRATCH7	Scratch register
0x2c	TICK	Controls the tick generator

For more detailed information, please refer to section 4.7 Watchdog in the RP2040 datasheet.

4.9.8 RTC

The Real-Time Clock (RTC) provides time in a human-readable format and can be used to generate interrupts at specific times.

The RTC registers start at a base address of 0x4005c000 (defined as RTC_BASE in SDK).

Table 14. List of RTC registers

Offset	Name	Info
0x00	CLKDIV_M1	Divider minus 1 for the 1 second counter
0x04	SETUP_0	RTC setup register 0
0x08	SETUP_1	RTC setup register 1
0x0c	CTRL	RTC Control and status
0x10	IRQ_SETUP_0	Interrupt setup register 0
0x14	IRQ_SETUP_1	Interrupt setup register 1
0x18	RTC_1	RTC register 1
0x1c	RTC_0	RTC register 0
0x20	INTR	Raw Interrupts
0x24	INTE	Interrupt Enable
0x28	INTF	Interrupt Force
0x2c	INTS	Interrupt status after masking & forcing

For more detailed information, please refer to section 4.8 RTC in the RP2040 datasheet.

4.9.9 ADC

The internal ADC of the W55RP20 is a 12-bit SAR ADC with a speed of 500ksps. It supports four GPIO inputs and one internal temperature sensor input, and it features sample FIFO, interrupt generation, and a DMA interface.

The ADC registers start at a base address of 0x4004c000 (defined as ADC_BASE in SDK).

Table 15. List of ADC registers

Offset	Name	Info
0x00	CS	ADC Control and Status
0x04	RESULT	Result of most recent ADC conversion
0x08	FCS	FIFO control and status
0x0c	FIFO	Conversion result FIFO
0x10	DIV	Clock divider
0x14	INTR	Raw Interrupts
0x18	INTE	Interrupt Enable
0x1c	INTF	Interrupt Force
0x20	INTS	Interrupt status after masking & forcing

For more detailed information, please refer to section 4.9 ADC in the RP2040 datasheet.

4.9.10 SSI

The W55RP20 includes an SSI controller on the QSPI pins, which communicates with flash memory and is part of the XIP block.

The SSI registers start at a base address of 0x18000000 (defined as XIP_SSI_BASE in SDK).

Table 16. List of SSI registers

Offset	Name	Info
0x00	CTRLR0	Control register 0
0x04	CTRLR1	Master Control register 1
0x08	SSIENR	SSI Enable
0x0c	MWCR	Microwire Control
0x10	SER	Slave enable
0x14	BAUDR	Baud rate
0x18	TXFTLR	TX FIFO threshold level
0x1c	RXFTLR	RX FIFO threshold level
0x20	TXFLR	TX FIFO level
0x24	RXFLR	RX FIFO level
0x28	SR	Status register
0x2c	IMR	Interrupt mask
0x30	ISR	Interrupt status
0x34	RISR	Raw interrupt status
0x38	TXOICR	TX FIFO overflow interrupt clear
0x3c	RXOICR	RX FIFO overflow interrupt clear
0x40	RXUICR	RX FIFO underflow interrupt clear
0x44	MSTICR	Multi-master interrupt clear
0x48	ICR	Interrupt clear
0x4c	DMACR	DMA control
0x50	DMATDLR	DMA TX data level
0x54	DMARDLR	DMA RX data level
0x58	IDR	Identification register
0x5c	SSI_VERSION_ID	Version ID
0x60	DR0	Data Register 0 (of 36)
0xf0	RX_SAMPLE_DLY	RX sample delay

0xf4	SPI_CTRLR0	SPI control
0xf8	TXD_DRIVE_EDGE	TX drive edge

For more detailed information, please refer to section 4.10 SSI in the RP2040 datasheet.

4.10 TCP/IP Offload Engine (TOE)

The W5500, part of the W55RP20, is an embedded internet solution from WIZnet, utilizing their Hardware TCP/IP technology. This single chip integrates TCP/IP protocol processing along with a 10/100 Ethernet PHY and MAC. Inside the W5500, there is full hardware logic and buffer memory capable of handling communication protocols such as TCP, UDP, IPv4, ICMP, IGMP, ARP, and PPPoE. Users can simultaneously operate up to 8 independent hardware sockets. The W5500 connects to an external MCU via an SPI interface. The SPI on the W5500 supports a maximum SPI main clock of 80MHz and offers a more efficient SPI protocol compared to previous products, enabling high-speed network communication. Additionally, to reduce system power consumption, the W5500 features low-power design, Wake On LAN (WOL), and Power Down modes.

- Support Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Support 8 independent sockets simultaneously
- Support Power down mode
- Support Wake on LAN over UDP
- Support High Speed Serial Peripheral Interface(SPI MODE 0, 3)
- Internal 32Kbytes Memory for TX/RX Buffers
- 10BaseT/100BaseTX Ethernet PHY embedded
- Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- Not support IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- LED outputs (Full/Half duplex, Link, Speed, Active)

For more detailed information, please refer to the [4]W5500 Datasheet.

[4] W5500 Datasheet Link : https://docs.wiznet.io/Product/iEthernet/W5500/datasheet

5 Mechanical standards

5.1 Packaging information

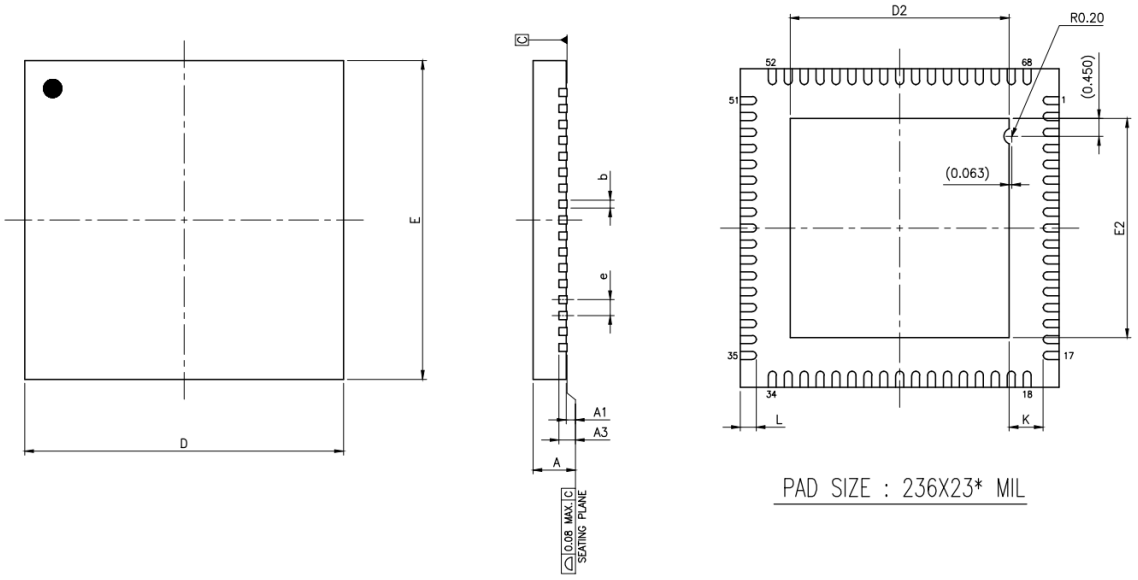

Figure 5. Package Dimensions

Table 17. QFN68 VARIATIONS

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.8	0.85	0.9	0.031	0.033	0.035
A1	0	0.02	0.05	0	0.001	0.002
A3		0.203 REF			0.008 REF	
b	0.15	0.2	0.25	0.006	0.008	0.01
D		8.00 BSC			0.315 BSC	
E		8.00 BSC			0.315 BSC	
e		0.40 BSC			0.016 BSC	
L	0.35	0.4	0.45	0.014	0.016	0.018
K	-0.2	-	-	-0.008	-	-
D2	6.15	6.2	6.25	0.242	0.244	0.246
E2	6.15	6.2	6.25	0.242	0.244	0.246

5.2 Recommended PCB Footprint

TBD

5.3 Solder profile

Moisture Sensitivity Level : 3
Dry Pack Required: Yes

Table 18. Solder profile values

Average Ramp-Up Rate (Ts_{max} to Tp)	3° C/second max.
Preheat - Temperature Min (Ts_{min}) - Temperature Max (Ts_{max}) - Time (tsmin to ts_{max})	 150 °C 200 °C 60-120 seconds
Time maintained above: - Temperature (TL) - Time (tL)	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	260 + 0/-5°C
Time within 5 °C of actual Peak Temperature (tp)	30 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

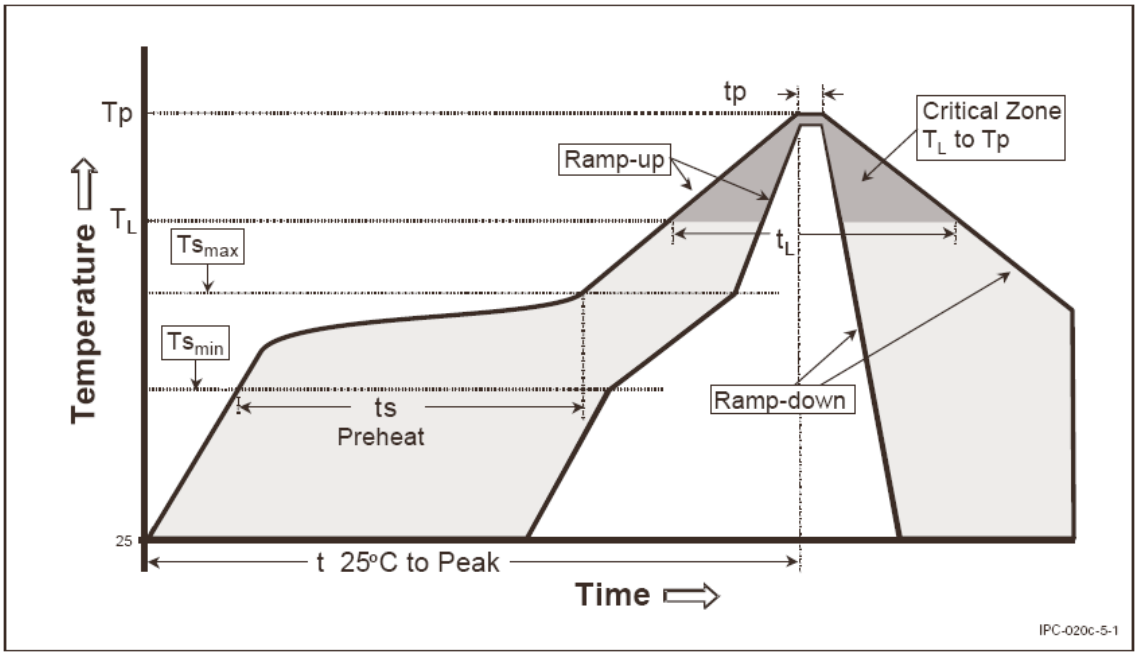

Figure 6. Classification profile (not to scale)

5.4 Electrical Characteristics

5.4.1 Absolute Maximum Ratings

Table 19. Absolute maximum ratings for digital IO and TOE block

Parameter	Symbol	Min	Max	Units	Comment
I/O Supply Voltage	IOVDD	-0.5	3.63	V	
Voltage at IO	V_{pin}	-0.5	IOVDD + 0.5	V	
TOE Digital Supply Voltage	VDD	-0.5	3.63	V	
TOE Analog Supply Voltage	AVDD	-0.5	3.63	V	

5.4.2 ESD Performance

Table 20. ESD performance for all pins, unless otherwise stated

Parameter	Symbol	Max	Units	Comment
Human Body Model	HBM	2	2kV	Compliant with JEDEC

				specification JS-001-2012 (April 2012)
Human Body Model Digital(FT) pins only	HBM	4	kV	Compliant with JEDEC specification JS-001-2012 (April 2012)
Charged Device Model	CDM	500	V	Compliant with JESD22-C101E (December 2009)

5.4.3 Thermal Performance

Table 21. Thermal Performance

Parameter	Symbol	Min	Typ	Max	Units	Comment
Case Temperature	T_C	-40		85	˚C	

5.4.4 GPIO Electrical Characteristics

Table 22. Digital IO characteristics - Standard and FT unless otherwise stated

Parameter	Symbol	Min	Max	Units	Comment
Pin Input Leakage	I_{IN}		1	uA	
Input Voltage High @ IOVDD-1.8V	V_{IH}	0.65 * IOVDD	IOVDD + 0.3	V	
Input Voltage High @ IOVDD-2.5V	V_{IH}	1.7	IOVDD + 0.3	V	
Input Voltage High @ IOVDD-3.3V	V_{IH}	2	IOVDD + 0.3	V	
Input Voltage Low @ IOVDD-1.8V	V_{IL}	-0.3	0.35 * IOVDD	V	
Input Voltage Low @ IOVDD-2.5V	V_{IL}	-0.3	0.7	V	
Input Voltage Low @ IOVDD-3.3V	V_{IL}	-0.3	0.8	V	
Input Hysteresis Voltage @ IOVDD=1.8V	V_{HYS}	0.1 * IOVDD		V	Schmitt Trigger enabled
Input Hysteresis Voltage @ IOVDD=2.5V	V_{HYS}	0.2		V	Schmitt Trigger enabled
Input Hysteresis Voltage @ IOVDD=3.3V	V_{HYS}	0.2		V	Schmitt Trigger enabled
Output Voltage High @ IOVDD=1.8V	V_{OH}	1.24	IOVDD	V	I_{OH} = 2, 4, 8 or 12mA depending on setting
Output Voltage High @ IOVDD=2.5V	V_{OH}	1.78	IOVDD	V	I_{OH} = 2, 4, 8 or 12mA depending on setting
Output Voltage High @ IOVDD=3.3V	V_{OH}	2.62	IOVDD	V	I_{OH} = 2, 4, 8 or 12mA depending on setting
Output Voltage Low @ IOVDD=1.8V	V_{OL}	0	0.3	V	I_{OL} = 2, 4, 8 or 12mA depending on setting

Output Voltage Low @ IOVDD=2.5V	V_{OL}	0	0.4	V	I_{OL} = 2, 4, 8 or 12mA depending on setting
Output Voltage Low @ IOVDD=3.3V	V_{OL}	0	0.5	V	I_{OL} = 2, 4, 8 or 12mA depending on setting
Pull-Up Resistance	R_{PU}		80	kΩ	
Pull-Down Resistance	R_{PD}		80	kΩ	
Maximum Total IOVDD current	I_{IOVDD_MAX}		50	mA	Sum of all current being sourced by GPIO and QSPI pins
Maximum Total VSS current due to IO (IOVSS)	I_{IOVSS_MAX}		50	mA	Sum of all current being sourced by GPIO and QSPI pins

Table 23. USB IO characteristics

Parameter	Symbol	Min	Max	Units	Comment
Pin Input Leakage Current	V_{IN}		1	uA	
Single Ended Input Voltage High	V_{IHSE}	2		V	
Single Ended Input Voltage Low	V_{ILSE}		0.8	V	
Differential Input Voltage High	V_{IHDIFF}	0.2		V	
Differential Input Voltage Low	V_{ILDIFF}		-0.2	V	
Output Voltage High	V_{OH}	2.8	USB_VDD	V	
Output Voltage Low	V_{OL}	0	0.3	V	
Pull-Up Resistance - RPU2	V_{PU2}	0.873	1.548	kΩ	
Pull-Up Resistance - RPU1&2	$V_{PU\&2}$	1.398	3.063	kΩ	
Pull-Down Resistance	V_{PD}	14.25	15.75	kΩ	

Table 24. ADC characteristics

Parameter	Symbol	Min	Max	Units	Comment
ADC Input Voltage Range	V_{PIN_ADC}	0	ADC_AVDD	V	
Effective Number of Bits	ENOB	8.7		Bits	See Section 4.9.3 of RP2040 Datasheet
Resolved Bits			12	Bits	
ADC Input Impedance	R_{IN_ADC}	100		kΩ	

Table 25. Oscillator pin characteristics when using a Square Wave input

Parameter	Symbol	Min	Max	Units	Comment
Input Voltage High	V_{IH}	0.65*IOVDD	IOVDD + 3	V	XIN only. XOUT floating
Input Voltage Low	V_{IL}	0	0.35*IOVDD	V	XIN only. XOUT floating

Table 26. TOE W5500 IO characteristics

Parameter	Symbol	Min	Typ	Max	Units	Comment
Pin Input Leakage	I_L			1	uA	
High level input voltage	V_{IH}	2.0		5.5	V	
Low level input voltage	V_{IL}	-0.3		0.8	V	
Pull-up Resistor	R_{PU}	62	77	112	kΩ	PMODE[2:0]
Low level output voltage @ I_{OL} = 8mA	V_{OL}			0.4	V	
High level output voltage @ I_{OH} = 8Ma	V_{OH}	2.4			V	
Low level output Current @ V_{OL} = 0.4V	I_{OL}	8.6	13.9	18.9	mA	
High level output Current @ V_{OH} = 0.4V	I_{OH}	12.5	26.9	47.1	Ma	

Table 27. TOE W5500 Crystal Characteristics

Parameter	Range
Frequency	25 MHz
Frequency Tolerance (at 25℃)	±30 ppm
Shunt Capacitance	7pF Max
Drive Level	59.12uW/MHz
Load Capacitance	18pF
Aging (at 25℃)	±3ppm / year Max

5.4.5 Power Supplies

Table 28. Power Supply Specifications

Power Symbol	Supplies	Min	Typ	Max	Units
IOVDD	MCU Digital IO	1.62	1.8 / 3.3	3.63	V
DVDD	MCU Digital Core	1.05	1.1	1.16	V
VREG_VIN	Voltage regulator	1.62	1.8 / 3.3	3.63	V
USB_VDD	USB PHY	3.135	3.3	3.63	V
ADC_AVDD	ADC	1.62	3.3	3.63	V
VDD, AVDD	TOE Digital & Analog	2.97	3.3	3.63	V

5.4.6 Power Consumption

TBD

5.4.7 Transformer Characteristics

Table 29. Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1	1:1
Inductance	350uH	350uH

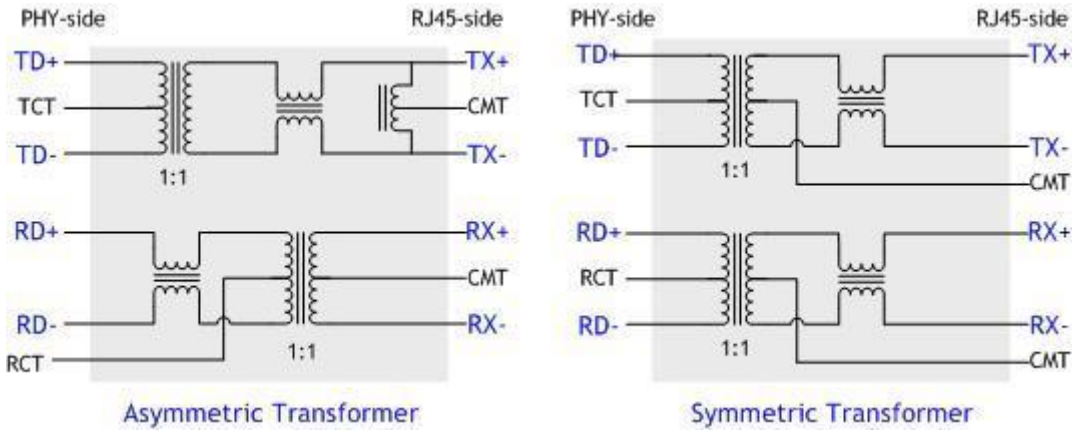

Figure 7. Transformer Type

5.4.8 MDIX

W55RP20 does not support auto-MDIX feature. Thus, user should use straight-through cables to connect to other switches or routers and crossover cables to connect to devices such as servers, workstations or another W55RP20. However, user can use either type of cable to connect to other devices with auto-MDIX enabled, and the interface automatically corrects for any incorrect cabling.

Document History Information

Version	Date	Descriptions
Ver 1.0.0	5-Mar-25	Initial Release
Ver 1.0.1	18-Dec-25	Updated maximum operating frequency (up to 133MHz → up to 133MHz (or 200MHz at 1.15V)
Ver 1.0.2	10-Feb-26	Added description of internal interface between RP2040 and W5500

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