W55MH32 Datasheet

Version 1.0.0

http://www.wiznet.io/

W55MH32

Enhanced, True Random Number, Hardware Encryption Algorithm Unit, 32-bit MCU with 1024KB Flash, 10/100 Ethernet MAC and PHY, Hardware Internet controller with an integrated full TCP/IP stack, USB, CAN, 17 Timers, 3 ADCs, 2 DACs, Up to 12 communication interface

Features:

- Encapsulation
  - W55MH32L:100QFN
  - W55MH32Q:68QFN
- Core: 32-bit Arm® Cortex®-M3 Core
  - Up to 216MHz operation frequency,2.54DMips/MHz(CoreMark1.0)
  - Single-cycle multiplication and hardware division
- Memories
  - 1024K bytes of Flash memory
  - 96Kbytes of SRAM
- Clock, reset and supply management
  - 2.0～3.6V application supply and I/Os
  - POR, PDR, and programmable voltage detector (PVD)
  - 4～16MHz crystal oscillator
  - Internal 8MHz factory-trimmed RC
  - Internal 40kHz RC oscillator with calibration
  - 32kHz RTC oscillator with calibration
- Low-power
  - Sleep, Stop and Standby modes
  - supply for RTC and backup registers
- 3 x 12-bit, 1 μs A/D converters (up to 12 channels)
  - Conversion range: 0 to 3.6V
  - Temperature sensor
- 2 x 12-bit D/A converters
- DMA：12-channel DMA controller
- Ethernet：10/100M Ethernet MAC and PHY
  - Supports following Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
  - Supports 8 independent sockets simultaneously
  - Internal 32Kbytes Memory for Tx/Rx Buffers
  - 10BaseT/100BaseTX Ethernet PHY embedded
  - Support Auto Negotiation (Full and half duplex, 10 and 100-based)
- LED outputs (Full/Half duplex, Link,Speed, Active)
- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Embedded Tracking Module(ETM)
- I/O ports
  - 66(W55MH32L) / 36(W55MH32Q) multi-function bidirectional I/O ports, all mappable on 16 external interrupts
  - All GPIOs can be forced to configure pull-up and pull-down resistors
- Enhanced CRC calculation unit
- 17 Timers
  - 10 x 16-bit timers, each with up to 4 input
  - capture/output compare/PWM or pulse counter
  - and quadrature (incremental) encoder input
  - 2 x 16-bit, advanced motor control PWM timer with dead-time generation and emergency stop
  - 2 watchdog timers (Independent and Window)
  - SysTick timer 24-bit downcounter
  - 2 x 16-bit base timers
- Up to 12 communication interface
  - Up to 2 x I2C interfaces(support SMBus/PMBus)
  - Up to 5(W55MH32L) / 3(W55MH32Q) x USARTs
  - Up to 2 SPI interfaces, 1 multiplexed with I2S interface
  - CAN interface(2.0B Active)
  - USB 2.0 full-speed interface(Optional internal
  - 1.5K pull-up resistor)
  - SDIO interface(only W55MH32L)
- Hardware encryption algorithm unit
  - Built-in hardware algorithm(DES、AES、SHA)
  - Provide a complete high-performance algorithm library
- TRNG：generate sequence of true random numbers
  - Four independent true random sources, which can be configured individually
  - 128BIT random numbers can be generated at
  - one time
  - Optional digital post-processing function
  - Attack detection
- SENSOR：voltage & temperature sensor alarm
  - VBAT and VDD voltage can be detected independently
  - Provide temperature detection sensor
  - Optional reset or interrupt after alarm
- SRAM scrambling
  - Support address and data scrambling
- One Time Programmable (OTP)
  - Support 32 Byte

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Introduction

This datasheet includes: the basic configuration of W55MH32(such as the capacity of built-in Flash and RAM, the type and quantity of peripheral modules, etc.), the number and assignment of pins, electrical characteristics, package information, etc.

1 Specification

1.1 Device overview

Table 1 Device Function Configuration Table

Family		W55MH32L	W55MH32Q
Flash(Kbytes)		1024	1024
SRAM(Kbytes)		96	96
Timers	Advanced	2	2
	General-purpose	10	10
	Basic	2	2
Communication	SPI	2	2
	I2C	2	2
	USART/UART	5	3
	USB	1	1
	CAN	1	1
	SDIO	1	-
	Ethernet	1	1
GPIO PORT		66	36
12bit ADC (number of channels)		3(12channels)	3(12channels)
12bit DAC (number of channels)		2(2channels)	2(2channels)
True Random Number Module		Support	Support
Hardware Encryption Algorithm Unit		Support	Support
Page size (Kbytes)		4	4
CPU frequency		216M	216M
Operating voltage		2.0~3.6V	2.0~3.6V
Operating temperature		-40 to +85℃	-40 to +85℃

1.2 Introduction

1.2.1 32-bit Arm® Cortex®-M3 Core

The 32-bit Arm® Cortex®-M3 core provides a cost-effective platform for meeting MCU requirements by reducing pin count and lowering system power consumption, while delivering exceptional computational performance and advanced interrupt system responsiveness.

1.2.2 TCP/IP Offload Engine (TOE)

Brief introduction

The TCP/IP Offload Engine (TOE) is an embedded all-hardware TCP/IP Ethernet controller, which can provide a more concise embedded network access solution. TOE technology enables users to use the hardware TCP/IP protocol stack to implement network access applications.

WIZnet all-hardware TCP/IP stack solution has been proven in many applications for many years, supporting TCP, UDP, IPv4, ICMP, ARP, IGMP and PPPoE protocols. The TOE embeds 32KB of internal cache for Ethernet packet processing.

The application of TOE technology allows users to implement Ethernet applications with some simple socket programming. Compared to other Ethernet solutions, this solution is faster and easier. Eight independent hardware socket can be used independently. At the same time, the TOE provides a WOL (Wake on LAN) function to reduce system power consumption.

Features

- Support full hardware TCP/IP protocols: TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Support 8 independent ports (Socket) simultaneous communication
- Support power-down mode
- Wake on LAN support
- Independent 32K byte transceiver cache
- 10BaseT/100BaseTX Ethernet PHY
- Support auto-negotiation

1.2.3 Embedded Flash memory

Embedded Flash is available for storing programs and data.

Table 2 Supply voltage and Flash Delay level matching table

Flash Delay Level	HCLK(MHz)	
	Voltage Range	Voltage Range
	2.3V - 3.6V	2.0V - 2.3V
0	0 < HCLK <= 108	0 < HCLK <= 32
1	108 < HCLK <= 216	32 < HCLK <= 64
2	-	64 < HCLK <= 128
3	-	128 < HCLK <= 192
4	-	192 < HCLK <= 216

1.2.4 Memory Protection Unit(MPU)

The Memory Protection Unit (MPU) manages CPU access to memory, preventing one task from accidentally corrupting memory or resources used by another active task. This memory area is organized into up to 8 protected areas, which can in turn be subdivided into up to 8 sub-areas. The protected area size can range from 32 bytes to the entire 4 Gbytes of addressable memory.

MPUs are especially useful in applications where some critical or certified code must be protected from misbehavior by other tasks. It is usually managed by RTOS (Real Time Operating System). If a program accesses a memory location that is restricted by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the settings of the MPU area based on the executing process.

1.2.5 Embedded SRAM

Up to 96 KB of built-in SRAM, accessible by the CPU with zero wait states for read and write operations.

1.2.6 CRC (cyclic redundancy check) calculation unit

The CRC (Cyclic Redundancy Check) calculation unit uses a fixed polynomial generator (with multiple selectable modes and hardware data processing) to generate a CRC code from a 32-bit data word.

In various applications, CRC-based techniques are used to verify the integrity of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, it provides a means for detecting flash memory errors.

1.2.7 Nested vectored interrupt controller (NVIC)

8 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support interrupt tail-chaining function
- Processor state automatically saved
- Interrupt entry restored on interrupt exit without additional instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

1.2.8 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period.

1.2.9 Clocks and startup

The system clock selection is performed at startup. Upon reset, the internal 8 MHz RC oscillator is chosen as the default CPU clock. Subsequently, an external 4–16 MHz clock with failure monitoring can be selected. If the external clock fails, it is isolated and the system automatically switches to the internal RC oscillator. If interrupts are enabled, the software can receive the corresponding interrupt. Similarly, comprehensive interrupt management for the PLL clock can be enabled when needed, such as when an indirectly utilized external oscillator fails.

Multiple prescalers are available to configure the frequencies of the AHB, high-speed APB (APB2), and low-speed APB (APB1) domains. The maximum frequency for AHB and high-speed APB is 216 MHz, while the maximum frequency for low-speed APB is 108 MHz.

1.2.10 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from program flash memory
- Boot from System Memory
- Boot from embedded SRAM

The Bootloader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

1.2.11 Power supply schemes

- VDD: Power supply for I/O pins and internal voltage regulator.
- VSSA, VDDA: Provide power for analog part of ADC, reset module, RC oscillator and PLL. VDDA and VSSA must be connected to VDD and VSS, respectively.
- VBAT: Backup power supply for RTC, external clock 32 kHz oscillator and backup registers (through internal power switch) when VDD is turned off.

  Note: Refer to the general operating conditions for each voltage range

1.2.12 Power supply supervisor

W55MH32 integrates an internal Power-On Reset (POR) and Power-Down Reset (PDR) circuit, which remains active at all times to ensure system operates when the supply voltage exceeds 2V. If VDD drops below the preset threshold (VPOR/PDR), the device is forced into a reset state without requiring an external reset circuit.

Additionally, it features a programmable voltage detector (PVD) that monitors the VDD/VDDA supply and compares it with the threshold VPVD. If VDD falls below or rises above VPVD, an interrupt is triggered. The interrupt handler can issue a warning or switch the microcontroller into a safe mode. The PVD function must be enabled through software.

1.2.13 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR mode is used for normal operation.
- LPR mode is used for the stop mode of CPU
- Power down mode is used for CPU standby mode: the regulator output is in a high-impedance state, power to the core circuits is cut off and the regulator enters a zero-power state (however, register and SRAM contents will be lost)

The regulator remains active after reset and is turned off in standby mode, entering a high-impedance output state.

1.2.14 Low-power modes

- Sleep mode

In Sleep mode, only the CPU stops while all peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

Stop mode achieves the lowest power consumption while preserving SRAM and register contents. In this mode, it cuts off the power supply to all internal 1.1V domains. Additionally, the PLL, HSI RC oscillator, and HSE crystal oscillator are disabled. The regulator can be set to either normal mode or low-power mode.

The microcontroller can be awakened from stop mode by any signal configured as an EXTI signal. These EXTI signals include one of the 16 external I/O pins, the PVD output, the RTC alarm, or a USB wake-up signal.

- Standby mode

Standby mode achieves the lowest power consumption. The internal voltage regulator is turned off and cuts the power to all internal 1.1V domains. Additionally, the PLL, HSI RC oscillator, and HSE crystal oscillator are disabled. Upon entering standby mode, SRAM and register contents are lost, but backup register contents remain preserved and the standby circuitry remains operational.

Exit from standby mode can be triggered by an external reset signal on NRST, an IWDG reset, a rising edge on a WKUP pin or an RTC alarm timeout.

Note: When entering shutdown or standby mode, the RTC, IWDG, and their respective clocks remain active.

1.2.15 DMA

Supports up to 12 general-purpose DMA channels (DMA1 with 7 channels, DMA2 with 5 channels) for managing data transfers between memory and memory, peripherals and memory, and memory and peripherals. The DMA controller supports circular buffer management, preventing interrupts when a transfer reaches the buffer's end.

Each channel has dedicated hardware DMA request logic and can also be triggered by software. The transfer length, source address, and destination address can all be configured independently via software.

DMA can be used with major peripherals, including SPI/I2S, I2C, USART, advanced/general-purpose/basic timers (TIMx), ADC, DAC, and SDIO.

1.2.16 RTC (real-time clock) and backup registers

The RTC and backup registers are powered through a switch. When VDD is available, the switch selects VDD as the power source; otherwise, power is supplied from the VBAT pin. The backup registers (42 16-bit registers) can store up to 84 bytes of user application data when VDD is turned off. Neither the RTC nor the backup registers are affected by system or power reset sources, and they remain intact when waking up from standby mode.

The real-time clock (RTC) features a continuously running counter that, with appropriate software, provides calendar clock functionality. It also supports alarm interrupts and periodic interrupts. The RTC can be driven by a 32.768 kHz oscillator using an external crystal, an internal low-power RC oscillator, or a high-speed external clock divided by 128. The internal low-power RC oscillator has a typical frequency of 40 kHz. To compensate for natural crystal deviations, the RTC clock can be calibrated using a 512 Hz output signal.

The RTC includes a 32-bit programmable counter, allowing long-duration measurements using a compare register. A 20-bit prescaler is used for the time base clock. By default, when the clock is set to 32.768 kHz, it generates a one-second time reference.

1.2.17 Timers and watchdogs

W55MH32series include at most 2 advanced-control timers, 10 general-purpose timers, 2 basic timers, 2 watchdog timers and 1 SysTick timer.

Following table compares the features of the advanced-control, general-purpose and basic timers.

Table 3 TIM configuration table

Timer	Counter Resolution	Counter Type	Prescaler Factor	Generate a DMA Request	Capture/Compare Channels	Complementary Outputs
TIM1 TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2 TIM3 TIM4 TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9 TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10 TIM11 TIM13 TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6 TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Advanced-control timer (TIM1 and TIM8)

The two advanced control timers (TIM1 and TIM8) can be regarded as three-phase PWM generators with six channels. They feature complementary PWM outputs with dead-time insertion and it can function as fully capable general-purpose timers.

The 4 independent channels can be used for

- Input capture
- Output comparison
- PWM generator (edge- or center-aligned modes)
- Signal pulse output

When configured as a general-purpose 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the counters can be frozen, and PWM outputs are disabled, effectively shutting off switches controlled by these outputs. Many features are identical to standard TIM timers, and they share the same internal structure. As a result, advanced control timers can operate in conjunction with TIM timers through the timer linkage function, enabling synchronization or event linking.

General-purpose timer(TIM2、TIM3、TIM4、TIM5)

There are up to four synchronizable general-purpose timers embedded in the W55MH32 devices.These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and 4 independent channels each for input capture/output compare, PWM or single-pulse mode output. The general-purpose timers can work together with the advanced-control timer via the Timer Link feature for synchronization or chaining events. These counters can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

These timers are also capable of processing incremental encoder signals as well as digital outputs from 1 to 3 hall-effect sensors.

General-purpose timer(TIM10、TIM11、TIM9)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM10 and TIM11 have one independent channel, while TIM9 has two independent channel outputs for input capture/output comparison, PWM or single-pulse output. They can fully synchronize general purpose timers with TIM2, TIM3, TIM4, TIM5. They can also be used as a simple time base.

General-purpose timer(TIM13、TIM14、TIM12)

These timers are based on a 16-bit auto-reload counter and a 16-bit prescaler. TIM13 and TIM14 have one independent channel, while TIM12 has two independent channels outputs for input capture/output comparison, PWM or single-pulse output. They can fully synchronize general purpose timers with TIM2, TIM3, TIM4, TIM5. They can also be used as a simple time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40kHz internal RC. As it operates independently with the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the system when a problem occurs, or as a free-running timer for application timeout management. The watchdog can be configured to start via software or hardware through option bytes. The counter can be frozen in debug mode.

Basic timer TIM6 and TIM7

These timers are mainly used for the generating of DAC triggers. They can also be used as a universal 16-bit time base.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the system when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

1.2.18 I2C bus

Up to two I2C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes. The I2C interface supports 7-bit or 10-bit addressing, and the 7-bit slave mode supports dual-slave addressing. A hardware CRC generation /verification is embedded.

They can be served by DMA and they support SM Bus 2.0/PM Bus.

1.2.19 Universal synchronous/asynchronous receiver transmitter (USART)

Three universal synchronous/asynchronous receiver transmitter(USART1, USART2 and USART3) and two universal asynchronous receiver transmitter(UART4 and UART5).The five interfaces provide asynchronous communication, IrDA SIR ENDEC support,Multi-processor communication mode, single-line semi-duplex communication mode and LIN Master/Slave capability.

USART1 interface communication rate can reach 13.5Mbits/s.

USART1, USART2 and USART3 provide hardware management of the CTS and RTS signals, are compliant with ISO7816 smart card mode and SPI-like communication mode.

1.2.20 Serial peripheral interface (SPI)

Up to 2 SPI interfaces. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

1.2.21 Audio Interface (I2S)

A standard I2S interface (multiplexed with SPI3) can operate in either master or slave mode. This interface supports 16-bit or 32-bit data transmission and can be configured as either an input or output channel. It supports audio sampling frequencies ranging from 8 kHz to 48 kHz. When configured in master mode, the I2S interface can output a master clock at 256 times the sampling frequency to an external DAC or CODEC (decoder).

1.2.22 SDIO

The SD/SDIO/MMC host interface can support 3 different data bus modes in the MMC Card System Specification 4.2: 1-bit (default), 4-bit, and 8-bit. SDIO Memory Card Specification 2.0 supports two data bus modes: 1-bit (default) and 4-digit. The current chip version can only support one SD/SDIO/MMC version 4.2 card at a time but can simultaneously support multiple MMC version 4.1 or early version cards.

In In addition to SD/SDIO/MMC, this interface is fully compatible with the CE-ATA digital protocol version 1.1.

1.2.23 Controller area network (CAN)

The CAN interface supports protocol of 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifier as well as extended frames with 29-bit identifier. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

1.2.24 Universal serial bus (USB)

Embedded a full-speed USB device controller, follows the full-speed USB device (12m/s) standard. The endpoint can be configured by software and includes standby/wake-up features. The USB dedicated 48MHz clock is directly generated by the internal master PLL (with a selectable clock source).

1.2.25 General-purpose inputs/outputs (GPIO)

Each GPIO pin can be configured via software as an output (push-pull or open-drain), an input (with or without pull-up or pull-down), or as a multiplexed peripheral function. Most GPIO pins are shared with digital or analog peripheral functions. Except for ports with analog input functionality, all GPIO pins support high-current drive capability.

When necessary, the peripheral function of an I/O pin can be locked through a specific operation to prevent unintended writes to the I/O registers. Additionally, each I/O can be configured with internal pull-up or pull-down resistors, reducing the need for external resistors.

1.2.26 Analog-to-digital converter (ADC)

Supports up to three 12-bit Analog-to-Digital Converters (ADCs) with up to 12 external channels, capable of single or scan conversions. In scan mode, conversions are

automatically performed on a selected group of analog inputs.

Additional logic functions available on the ADC interface include:

- Synchronized sampling and hold
- Interleaved sampling and hold
- Single sampling

The ADC can operate with DMA for efficient data transfer.

The analog watchdog function enables highly precise monitoring of one, multiple, or all selected channels. If the monitored signal exceeds a predefined threshold, an interrupt is triggered.

Events generated by standard timers (TIMx) and advanced control timers (TIM1 and TIM8) can be internally cascaded to the ADC for start and injected triggers, allowing applications to synchronize AD conversions with the system clock.

1.2.27 Digital-to-analog converter (DAC)

The two 12-bit buffered DAC channels can convert two digital signals into two analog voltage outputs.

This dual digital interface supports the following features:

- Two DAC converters, each with a dedicated output channel
- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update functionality
- Noise wave generation
- Triangle wave generation
- Independent or synchronized conversion of both DAC channels
- DMA functionality available for each channel
- External trigger for conversion
- Input reference voltage **V_REF+**

The DAC channels can be triggered by the update output of a timer, which can also be connected to different DMA channels.

1.2.28 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC11_IN16 input channel which is used to convert the sensor output voltage into a digital value

1.2.29 Serial wire JTAG debug port(SWJ-DP)

The embedded SWJ-DP interface combines JTAG and Serial Wire Debug (SWD), allowing connection via either the Serial Wire Debug interface or the JTAG interface. The JTAG TMS and TCK signals share pins with SWDIO and SWCLK, respectively. A specific signal sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

1.2.30 Embedded Tracking Module (ETM)

Using the Embedded Trace Macrocell (ETM), a high-speed compressed data stream can be output from the CPU core through a minimal number of ETM pins to an external Trace Port Analyzer (TPA) device. This provides developers with clear insights into instruction execution and data flow.

The TPA device can connect to the debugging host via USB, Ethernet, or other high-speed channels. Real-time instruction and data flow can be recorded by debugging software on the host and displayed in the desired format. TPA hardware is available from development tool vendors and is compatible with third-party debugging software.

1.2.31 True random number generator (TRNG)

The TRNG (True Random Number Generator) unit is used to generate a sequence of true random numbers. Each operation produces a 128-bit true random number sequence. It can be configured to generate a CPU interrupt request after random number generation.

2 Pinouts and pin description

2.1 W55MH32L

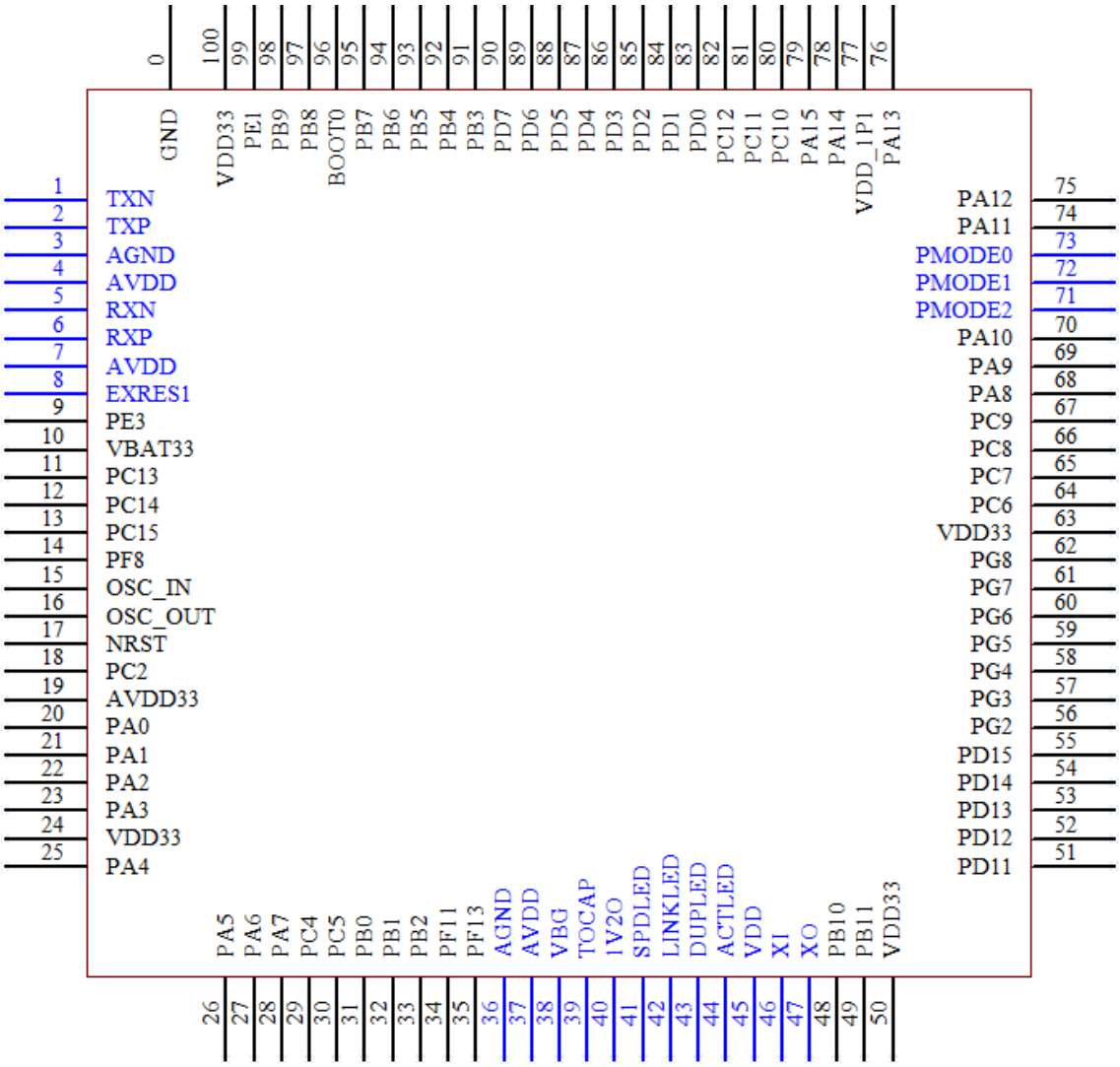


Figure 1 W55MH32L package

Table 4 W55MH32L pin description

NO	Pin Name	Type	I/O Level	Main Function (after reset)	Default/ Description	Remap
1	TXN	AO	-	TXN	**TXP/TXN Signal Pair** The differential data is transmitted to the media on the TXP/TXN signal pair.	-
2	TXP	AO	-	TXP		-
3	AGND	AGND	-	-	Analog ground of ethernet	-
4	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
5	RXN	AI	-	RXN	**RXP/RXN Signal Pair** The differential data from the media is received on the RXP/RXN signal pair.	-
6	RXP	AI	-	RXP		-
7	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
8	EXRES	-	-	-	**External Reference Resistor** It should be connected to an external resistor (12.4KΩ, 1%) needed for biasing of internal analog circuits.	-
9	PE3	-	-	-	-	-
10	VBAT	VBAT	S	-	VBAT	-
11	PC13-TAMPERRTC	I/O	-	PC13	TAMPER-RTC	-

NO	Pin Name	Type	I/O Level	Main Function (after reset)	Default/ Description	Remap
12	PC14-OSC32_IN	I/O	-	PC14	OSC32_IN	-
13	PC15-OSC32_OUT	I/O	-	PC15	OSC32_OUT	-
14	PF8	I/O	-	PF8	ADC3_IN6	-
15	OSC_IN	I	-	OSC_IN	-	-
16	OSC_OUT	O	-	OSC_OUT	-	-
17	nRESET	I	-	nRESET	-	-
18	PC2	I/O	-	PC2	ADC123_IN12	-
19	VDDA	PWR	-	-	-	-
20	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR/ TIM5_CH1/TIM8_ETR	-
21	PA1	I/O	-	PA1	USART2_RTS/ADC123_IN1/ TIM2_CH2/TIM5_CH2	-
22	PA2	I/O	-	PA2	USART2_TX/ADC123_IN2/ TIM2_CH3/TIM5_CH3/ TIM9_CH1	-
23	PA3	I/O	-	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
24	VDD	PWR	-	-	-	
25	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
26	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5/ DAC_OUT2	-
27	PA6	I/O	-	PA6	SPI1_MISO/ADC12_IN6/ TIM3_CH1/TIM8_BKIN/ TIM13_CH1	TIM1_BKIN
28	PA7	I/O	-	PA7	SPI1_MOSI/ADC12_IN7/ TIM3_CH2/TIM8_CH1N/ TIM14_CH1	TIM1_CH1N
29	PC4	I/O	-	PC4	ADC12_IN14	-
30	PC5	I/O	-	PC5	ADC12_IN15	-
31	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3/ TIM8_CH2N	TIM1_CH2N
32	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4/ TIM8_CH3N	TIM1_CH3N
33	PB2	I/O	FT	PB2/BOOT1	-	-
34	PF11	I/O	FT	PF11	-	-
35	PF13	I/O	FT	PF13	-	-
36	AGND	AGND	-	-	Analog ground of ethernet	-
37	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
38	VBG	AO	-	-	**Band Gap Output Voltage** This pin will be measured as 1.2V at 25℃. It must be left floating	-
39	TOCAP	AO	-	-	**External Reference Capacitor** This pin must be connected to a 4.7uF capacitor. The trace length to the capacitor should be short to stabilize the internal signals.	-
40	1V2O	PWR	-	-	**1.2V Regulator output voltage** A 10nF capacitor must be connected to this pin This is the output voltage of the internal regulator	-
41	SPDLED	O	-	SPDLED	**Speed LED** This shows the Ethernet Speed status of the connected link. Low: 100Mbps High: 10Mbps	-
42	LINKLED	O	-	LINKLED	**Link LED** This shows the Ethernet Link status. Low: Link is established High: Link is not established	-
43	DUPLED	O	-	DUPLED	**Duplex LED** This shows the Ethernet Duplex status for the connected link. Low: Full-duplex mode High: Half-duplex mode	-
44	ACTLED	O	-	ACTLED	**Active LED** This shows that there is Carrier sense (CRS) from the active Physical Medium Sub-layer (PMD) during TX or RX activity. Low: Carrier sense from the active PMD High: No carrier sense	
45	VCC33	PWR	-	-	Digital 3.3V Power of ethernet department	-
46	XI	AI	-	-	**Crystal input / External Clock input** External 25MHz Crystal Input. This pin can also be connected to single-ended TTL oscillator (CLKIN). 3.3V clock should be applied for the External Clock input. If this method is implemented, XO should be left unconnected.	-
47	XO	AO	-	-	**Crystal output** External 25MHz Crystal Output Note: Float this pin if using an external clock being driven through XI/CLKIN	-
48	PB10	I/O	FT	PB10	I2C2_SCL/USART3_TX	TIM2_CH3

<table>
<tr><th>NO</th><th>Pin Name</th><th>Type</th><th>I/O Level</th><th>Main Function (after reset)</th><th>Default/ Description</th><th>Remap</th></tr>
<tr><td>49</td><td>PB11</td><td>I/O</td><td>FT</td><td>PB11</td><td>I2C2_SDA/USART3_RX</td><td>TIM2_CH4</td></tr>
<tr><td>50</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>51</td><td>PD11</td><td>I/O</td><td>FT</td><td>PD11</td><td>-</td><td>-</td></tr>
<tr><td>52</td><td>PD12</td><td>I/O</td><td>FT</td><td>PD12</td><td>-</td><td>TIM4_CH1
/USART3_RX</td></tr>
<tr><td>53</td><td>PD13</td><td>I/O</td><td>FT</td><td>PD13</td><td>-</td><td>TIM4_CH2</td></tr>
<tr><td>54</td><td>PD14</td><td>I/O</td><td>FT</td><td>PD14</td><td>-</td><td>TIM4_CH3</td></tr>
<tr><td>55</td><td>PD15</td><td>I/O</td><td>FT</td><td>PD15</td><td>-</td><td>TIM4_CH4</td></tr>
<tr><td>56</td><td>PG2</td><td>I/O</td><td>FT</td><td>PG2</td><td>-</td><td>-</td></tr>
<tr><td>57</td><td>PG3</td><td>I/O</td><td>FT</td><td>PG3</td><td>-</td><td>-</td></tr>
<tr><td>58</td><td>PG4</td><td>I/O</td><td>FT</td><td>PG4</td><td>-</td><td>-</td></tr>
<tr><td>59</td><td>PG5</td><td>I/O</td><td>FT</td><td>PG5</td><td>-</td><td>-</td></tr>
<tr><td>60</td><td>PG6</td><td>I/O</td><td>FT</td><td>PG6</td><td>-</td><td>-</td></tr>
<tr><td>61</td><td>PG7</td><td>I/O</td><td>FT</td><td>PG7</td><td>-</td><td>-</td></tr>
<tr><td>62</td><td>PG8</td><td>I/O</td><td>FT</td><td>PG8</td><td>-</td><td>-</td></tr>
<tr><td>63</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>64</td><td>PC6</td><td>I/O</td><td>FT</td><td>PC6</td><td>TIM8_CH1/SDIO_D6</td><td>TIM3_CH1</td></tr>
<tr><td>65</td><td>PC7</td><td>I/O</td><td>FT</td><td>PC7</td><td>I2S3_MCK/TIM8_CH2/
SDIO_D7</td><td>TIM3_CH2</td></tr>
<tr><td>66</td><td>PC8</td><td>I/O</td><td>FT</td><td>PC8</td><td>TIM8_CH3/SDIO_D0</td><td>TIM3_CH3</td></tr>
<tr><td>67</td><td>PC9</td><td>I/O</td><td>FT</td><td>PC9</td><td>TIM8_CH4/SDIO_D1</td><td>TIM3_CH4</td></tr>
<tr><td>68</td><td>PA8</td><td>I/O</td><td>FT</td><td>PA8</td><td>USART1_CK/TIM1_CH1/MCO</td><td>-</td></tr>
<tr><td>69</td><td>PA9</td><td>I/O</td><td>FT</td><td>PA9</td><td>USART1_TX/TIM1_CH2</td><td>-</td></tr>
<tr><td>70</td><td>PA10</td><td>I/O</td><td>FT</td><td>PA10</td><td>USART1_RX/TIM1_CH3</td><td>-</td></tr>
<tr><td>71</td><td>PMODE2</td><td>I</td><td>-</td><td>-</td><td rowspan="3">PHY Operation mode select pins
These pins determine the network mode. Refer to the below table for details.
<table><tr><th colspan="3">PMODE [2:0]</th><th rowspan="2">Description</th></tr><tr><th>2</th><th>1</th><th>0</th></tr><tr><td>0</td><td>0</td><td>0</td><td>10BT Half-duplex, Auto-negotiation disabled</td></tr><tr><td>0</td><td>0</td><td>1</td><td>10BT Full-duplex, Auto-negotiation disabled</td></tr><tr><td>0</td><td>1</td><td>0</td><td>100BT Half-duplex, Auto-negotiation disabled</td></tr><tr><td>0</td><td>1</td><td>1</td><td>100BT Full-duplex, Auto-negotiation disabled</td></tr><tr><td>1</td><td>0</td><td>0</td><td>100BT Half-duplex, Auto-negotiation enabled</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Not used</td></tr><tr><td>1</td><td>1</td><td>1</td><td>All capable, Auto-negotiation enabled</td></tr></table></td><td rowspan="3">-</td></tr>
<tr><td>72</td><td>PMODE1</td><td>I</td><td>-</td><td>-</td></tr>
<tr><td>73</td><td>PMODE0</td><td>I</td><td>-</td><td>-</td></tr>
<tr><td>74</td><td>PA11</td><td>I/O</td><td>-</td><td>PA11</td><td>USART1_CTS/USBDM
CAN_RX/TIM1_CH4</td><td>-</td></tr>
<tr><td>75</td><td>PA12</td><td>I/O</td><td>-</td><td>PA12</td><td>USART1_RTS/USBDP/
CAN_TX/TIM1_ETR</td><td>-</td></tr>
<tr><td>76</td><td>PA13</td><td>I/O</td><td>FT</td><td>JTMS-SWDIO</td><td>-</td><td>PA13</td></tr>
<tr><td>77</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>78</td><td>PA14</td><td>I/O</td><td>FT</td><td>JTCK-SWCLK</td><td>-</td><td>PA14</td></tr>
<tr><td>79</td><td>PA15</td><td>I/O</td><td>FT</td><td>JTDI</td><td>SPI3_NSS/I2S3_WS</td><td>TIM2_CH1_ETR/
PA15/SPI1_NSS</td></tr>
<tr><td>80</td><td>PC10</td><td>I/O</td><td>FT</td><td>PC10</td><td>UART4_TX/SDIO_D2</td><td>USART3_TX</td></tr>
<tr><td>81</td><td>PC11</td><td>I/O</td><td>FT</td><td>PC11</td><td>UART4_RX/SDIO_D3</td><td>USART3_RX</td></tr>
<tr><td>82</td><td>PC12</td><td>I/O</td><td>FT</td><td>PC12</td><td>UART5_TX/SDIO_CK</td><td>USART3_CK</td></tr>
<tr><td>83</td><td>PD0</td><td>I/O</td><td>FT</td><td>PD0</td><td>-</td><td>CAN_RX</td></tr>
<tr><td>84</td><td>PD1</td><td>I/O</td><td>FT</td><td>PD1</td><td>-</td><td>CAN_TX</td></tr>
<tr><td>85</td><td>PD2</td><td>I/O</td><td>FT</td><td>PD2</td><td>TIM3_ETR/UART5_RX
SDIO_CMD</td><td>-</td></tr>
<tr><td>86</td><td>PD3</td><td>I/O</td><td>FT</td><td>PD3</td><td>-</td><td>USART2_CTS</td></tr>
<tr><td>87</td><td>PD4</td><td>I/O</td><td>FT</td><td>PD4</td><td>-</td><td>USART2_RTS</td></tr>
<tr><td>88</td><td>PD5</td><td>I/O</td><td>FT</td><td>PD5</td><td>-</td><td>USART2_TX</td></tr>
<tr><td>89</td><td>PD6</td><td>I/O</td><td>FT</td><td>PD6</td><td>-</td><td>USART2_RX</td></tr>
<tr><td>90</td><td>PD7</td><td>I/O</td><td>FT</td><td>PD7</td><td>-</td><td>-</td></tr>
<tr><td>91</td><td>PB3</td><td>I/O</td><td>FT</td><td>JTDO</td><td>SPI3_SCK/I2S3_CK</td><td>PB3/TRACESWO
TIM2_CH2/
SPI1_SCK</td></tr>
<tr><td>92</td><td>PB4</td><td>I/O</td><td>FT</td><td>NJTRST</td><td>SPI3_MISO</td><td>PB4/TIM3_CH1/
SPI1_MISO</td></tr>
<tr><td>93</td><td>PB5</td><td>I/O</td><td>-</td><td>PB5</td><td>I2C1_SMBA/SPI3_MOSI/I2S3_SD</td><td>TIM3_CH2/
SPI1_MOSI</td></tr>
<tr><td>94</td><td>PB6</td><td>I/O</td><td>FT</td><td>PB6</td><td>I2C1_SCL/TIM4_CH1</td><td>USART1_TX</td></tr>
<tr><td>95</td><td>PB7</td><td>I/O</td><td>FT</td><td>PB7</td><td>I2C1_SDA/TIM4_CH2</td><td>USART1_RX</td></tr>
<tr><td>96</td><td>BOOT0</td><td>I</td><td>-</td><td>BOOT0</td><td>-</td><td>-</td></tr>
<tr><td>97</td><td>PB8</td><td>I/O</td><td>FT</td><td>PB8</td><td>TIM4_CH3/SDIO_D4/TIM10_CH1</td><td>I2C1_SCL/CAN_RX</td></tr>
<tr><td>98</td><td>PB9</td><td>I/O</td><td>FT</td><td>PB9</td><td>TIM4_CH4/SDIO_D5/TIM11_CH1</td><td>I2C1_SDA/CAN_TX</td></tr>
<tr><td>99</td><td>PE1</td><td>I/O</td><td>FT</td><td>PE1</td><td>-</td><td>-</td></tr>
<tr><td>100</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
</table>

2.2 W55MH32Q

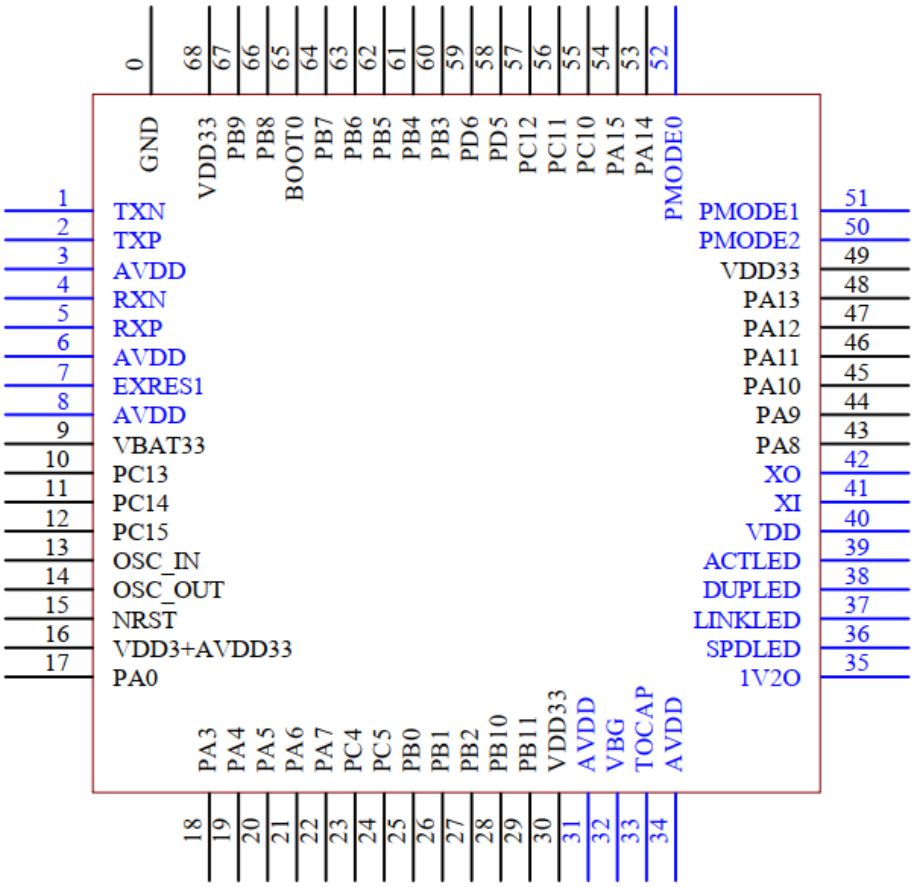


Figure 2 W55MH32Q package

Table 5 W55MH32Q pin description

NO	Pin Name	Type	I/O Level	Main Function (after reset)	Default/ Description	Remap
1	TXN	AO	-	TXN	**TXP/TXN Signal Pair** The differential data is transmitted to the media on the TXP/TXN signal pair.	-
2	TXP	AO	-	TXP		-
3	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
4	RXN	AI	-	RXN	**RXP/RXN Signal Pair** The differential data from the media is received on the RXP/RXN signal pair.	-
5	RXP	AI	-	RXP		-
6	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
7	EXRES	-	-	-	**External Reference Resistor** It should be connected to an external resistor (12.4KΩ, 1%) needed for biasing of internal analog circuits.	-
8	AVDD	PWR	-	-	Analog 3.3V power of ethernet	-
9	VBAT	VBAT	S	-	VBAT	-
10	PC13-TAMPERRTC	I/O	-	PC13	TAMPER-RTC	-
11	PC14-OSC32_IN	I/O	-	PC14	OSC32_IN	-
12	PC15-OSC32_OUT	I/O	-	PC15	OSC32_OUT	-
13	OSC_IN	I	-	OSC_IN	-	-
14	OSC_OUT	O	-	OSC_OUT	-	-
15	nRESET	I	-	nRESET	-	-
16	VDDA	PWR	-	-	-	-
17	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC123_IN0/TIM2_CH1_ETR/ TIM5_CH1/TIM8_ETR	-
18	PA3	I/O	-	PA3	USART2_RX/ADC123_IN3/ TIM2_CH4/TIM5_CH4/ TIM9_CH2	-
19	PA4	I/O	-	PA4	SPI1_NSS/USART2_CK/ DAC_OUT1/ADC12_IN4	-
20	PA5	I/O	-	PA5	SPI1_SCK/ADC12_IN5/	-

<table>
<tr><th>NO</th><th>Pin Name</th><th>Type</th><th>I/O Level</th><th>Main Function (after reset)</th><th>Default/ Description</th><th>Remap</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>DAC_OUT2</td><td></td></tr>
<tr><td>21</td><td>PA6</td><td>I/O</td><td>-</td><td>PA6</td><td>SPI1_MISO/ADC12_IN6/
TIM3_CH1/TIM8_BKIN/
TIM13_CH1</td><td>TIM1_BKIN</td></tr>
<tr><td>22</td><td>PA7</td><td>I/O</td><td>-</td><td>PA7</td><td>SPI1_MOSI/ADC12_IN7/
TIM3_CH2/TIM8_CH1N/
TIM14_CH1</td><td>TIM1_CH1N</td></tr>
<tr><td>23</td><td>PC4</td><td>I/O</td><td>-</td><td>PC4</td><td>ADC12_IN14</td><td>-</td></tr>
<tr><td>24</td><td>PC5</td><td>I/O</td><td>-</td><td>PC5</td><td>ADC12_IN15</td><td>-</td></tr>
<tr><td>25</td><td>PB0</td><td>I/O</td><td>-</td><td>PB0</td><td>ADC12_IN8/TIM3_CH3/
TIM8_CH2N</td><td>TIM1_CH2N</td></tr>
<tr><td>26</td><td>PB1</td><td>I/O</td><td>-</td><td>PB1</td><td>ADC12_IN9/TIM3_CH4/
TIM8_CH3N</td><td>TIM1_CH3N</td></tr>
<tr><td>27</td><td>PB2</td><td>I/O</td><td>FT</td><td>PB2/BOOT1</td><td>-</td><td>-</td></tr>
<tr><td>28</td><td>PB10</td><td>I/O</td><td>FT</td><td>PB10</td><td>I2C2_SCL/USART3_TX</td><td>TIM2_CH3</td></tr>
<tr><td>29</td><td>PB11</td><td>I/O</td><td>FT</td><td>PB11</td><td>I2C2_SDA/USART3_RX</td><td>TIM2_CH4</td></tr>
<tr><td>30</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>31</td><td>AVDD</td><td>PWR</td><td>-</td><td>-</td><td>Analog 3.3V power of ethernet</td><td>-</td></tr>
<tr><td>32</td><td>VBG</td><td>AO</td><td>-</td><td>-</td><td>Band Gap Output Voltage
This pin will be measured as 1.2V at 25℃. It must be left floating</td><td>-</td></tr>
<tr><td>33</td><td>TOCAP</td><td>AO</td><td>-</td><td>-</td><td>External Reference Capacitor
This pin must be connected to a 4.7uF capacitor. The trace length to the capacitor should be short to stabilize the internal signals.</td><td>-</td></tr>
<tr><td>34</td><td>AVDD</td><td>PWR</td><td>-</td><td>-</td><td>Analog 3.3V power of ethernet</td><td>-</td></tr>
<tr><td>35</td><td>1V2O</td><td>PWR</td><td>-</td><td>-</td><td>1.2V Regulator output voltage
A 10nF capacitor must be connected to this pin
This is the output voltage of the internal regulator</td><td>-</td></tr>
<tr><td>36</td><td>SPDLED</td><td>O</td><td>-</td><td>SPDLED</td><td>Speed LED
This shows the Ethernet Speed status of the connected link.
Low: 100Mbps
High: 10Mbps</td><td>-</td></tr>
<tr><td>37</td><td>LINKLED</td><td>O</td><td>-</td><td>LINKLED</td><td>Link LED
This shows the Ethernet Link status.
Low: Link is established
High: Link is not established</td><td>-</td></tr>
<tr><td>38</td><td>DUPLED</td><td>O</td><td>-</td><td>DUPLED</td><td>Duplex LED
This shows the Ethernet Duplex status for the connected link.
Low: Full-duplex mode
High: Half-duplex mode</td><td>-</td></tr>
<tr><td>39</td><td>ACTLED</td><td>O</td><td>-</td><td>ACTLED</td><td>Active LED
This shows that there is Carrier sense (CRS) from the active Physical Medium Sub-layer (PMD) during TX or RX activity.
Low: Carrier sense from the active PMD
High: No carrier sense</td><td></td></tr>
<tr><td>40</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>41</td><td>XI</td><td>AI</td><td>-</td><td>-</td><td>Crystal input / External Clock input
External 25MHz Crystal Input.
This pin can also be connected to single-ended TTL oscillator (CLKIN). 3.3V clock should be applied for the External Clock input. If this method is implemented, XO should be left unconnected.</td><td>-</td></tr>
<tr><td>42</td><td>XO</td><td>AO</td><td>-</td><td>-</td><td>Crystal output
External 25MHz Crystal Output
Note: Float this pin if using an external clock being driven through XI/CLKIN</td><td>-</td></tr>
<tr><td>43</td><td>PA8</td><td>I/O</td><td>FT</td><td>PA8</td><td>USART1_CK/TIM1_CH1/MCO</td><td>-</td></tr>
<tr><td>44</td><td>PA9</td><td>I/O</td><td>FT</td><td>PA9</td><td>USART1_TX/TIM1_CH2</td><td>-</td></tr>
<tr><td>45</td><td>PA10</td><td>I/O</td><td>FT</td><td>PA10</td><td>USART1_RX/TIM1_CH3</td><td>-</td></tr>
<tr><td>46</td><td>PA11</td><td>I/O</td><td>-</td><td>PA11</td><td>USART1_CTS/USBDM
CAN_RX/TIM1_CH4</td><td>-</td></tr>
<tr><td>47</td><td>PA12</td><td>I/O</td><td>-</td><td>PA12</td><td>USART1_RTS/USBDP/
CAN_TX/TIM1_ETR</td><td>-</td></tr>
<tr><td>48</td><td>PA13</td><td>I/O</td><td>FT</td><td>JTMS-SWDIO</td><td>-</td><td>PA13</td></tr>
<tr><td>49</td><td>VDD</td><td>PWR</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>50</td><td>PMODE2</td><td>I</td><td>-</td><td>-</td><td rowspan="2">PHY Operation mode select pins
These pins determine the network mode. Refer to the below table for details.</td><td>-</td></tr>
<tr><td>51</td><td>PMODE1</td><td>I</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>52</td><td>PMODE0</td><td>I</td><td>-</td><td>-</td><td>
<table>
<tr><th colspan="3">PMODE [2:0]</th><th rowspan="2">Description</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>10BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>100BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>100BT Half-duplex, Auto-negotiation enabled</td></tr>
</table>
</td><td>-</td></tr>
</table>

NO	Pin Name	Type	I/O Level	Main Function (after reset)	Default/ Description	Remap
					1 0 1 Not used 1 1 0 Not used 1 1 1 All capable, Auto-negotiation enabled	
53	PA14	I/O	FT	JTCK-SWCLK	-	PA14
54	PA15	I/O	FT	JTDI	SPI3_NSS/I2S3_WS	TIM2_CH1_ETR/ PA15/SPI1_NSS
55	PC10	I/O	FT	PC10	UART4_TX	USART3_TX
56	PC11	I/O	FT	PC11	UART4_RX	USART3_RX
57	PC12	I/O	FT	PC12	UART5_TX	USART3_CK
58	PD5	I/O	FT	PD5	-	USART2_TX
59	PD6	I/O	FT	PD6	-	USART2_RX
60	PB3	I/O	FT	JTDO	SPI3_SCK/I2S3_CK	PB3/TRACESWO TIM2_CH2/ SPI1_SCK
61	PB4	I/O	FT	NJTRST	SPI3_MISO	PB4/TIM3_CH1/ SPI1_MISO
62	PB5	I/O	-	PB5	I2C1_SMBA/SPI3_MOSI/I2S3_SD	TIM3_CH2/ SPI1_MOSI
63	PB6	I/O	FT	PB6	I2C1_SCL/TIM4_CH1	USART1_TX
64	PB7	I/O	FT	PB7	I2C1_SDA/TIM4_CH2	USART1_RX
65	BOOT0	I	-	BOOT0	-	-
66	PB8	I/O	FT	PB8	TIM4_CH3/TIM10_CH1	I2C1_SCL/CAN_RX
67	PB9	I/O	FT	PB9	TIM4_CH4/TIM11_CH1	I2C1_SDA/CAN_TX
68	VDD	PWR	-	-	-	-

3 Electrical characteristics

Parameter conditions

Unless otherwise specified, all voltages are referenced to VSS.

3.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and clock frequency by tests in production on 100% of the devices with an ambient temperature at TA = 25℃.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

3.2 Typical values

Unless otherwise specified, typical data are based on TA=25℃, VDD=3.3V.They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

3.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

Absolute maximum ratings

Loads placed on a device that exceed the values given in the 'Absolute Maximum Ratings' list may result in permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6 Voltage characteristics

Symbol	Description	Min	Max	Unit
VDD – VSS	External main supply voltage(including VDDA and VDD)(1)	-0.3	3.63	V
VIN	Input voltage on 5V tolerant pin(2)	Vss-0.3	Vdd+4.0	
	Input voltage on any other pin(2)	Vss-0.3	4.0	
|ΔVDDx|	Variations between different VDD power pins	—	50	mV
|VSSx-VSS|	Variations between all the different ground pins	—	50	

(1) All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

(2) Contains the VREF-feet.

Table 7 Current characteristics

Symbol	Description	Max (1)	Unit
IVDD	Total current into VDD/VDDA power lines (source) (1)	150	mA
IVSS	Total current out of VSS ground lines (sink) (1)	150	
IIO	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	-25	

(1) All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.

Table 8 Temperature characteristics

Symbol	Description	Value	Unit
TSTG	Storage temperature range	-65 ~ +150	℃
TJ	Maximum junction temperature	105	℃

Table 9 Electrostatic discharge (ESD) of Ethernet

Symbol	Parameter	Test Condition	Class	Maximum value(1)	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = +25 °C conforming to MIL-STD 883F Method 3015.7	2	2000	V
VESD(MM)	Electrostatic discharge voltage (man machine model)	TA = +25 °C conforming to JEDEC EIA/JESD22 A115-A	B	200	V
VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to JEDEC JESD22 C101-C	III	500	V

Table 10 Static latchup of Ethernet

Symbol	Parameter	Test Condition	Class	Maximum value(1)	Unit
LU	Static latch-up class	TA = +25 °C conforming to JESD78A	I	≥ ±200	mA

3.4 General operating conditions

Table 11 General operating conditions

Symbol	Parameter	Condition	Min	Max	Unit
fHCLK	Internal AHB clock frequency	—	0	216	MHz
fPCLK1	Internal APB1 clock frequency	—	0	108	
fPCLK2	Internal APB2 clock frequency	—	0	216	
VDD	Standard operating voltage	—	2.0	3.6	V
VDDA(1)	Analog part operating voltage	Must be same with VDD (1)	2.0	3.6	V
VBAT	Backup part operating voltage		1.6	3.6	V
TA	Ambient temperature	—	-40	85	℃

(1) It is recommended to power VDD and VDDA from the same source.

3.5 Operating conditions at power-up / power-down

The parameters given in the table below are based on the ambient temperature listed under the general operating conditions.

Table 12 Operating conditions at power-up / power-down

Symbol	Parameter	Condition	Min	Max	Unit
tVDD	VDD rise time rate	—	0	∞	us/V
	VDD fall time rate		20	∞	

3.6 Embedded reset and power control block characteristics

The parameters given in the table below are based on the VDD supply voltages listed under common operating conditions.

Table 13 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VPVD	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.16	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.07	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.26	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.17	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.35	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.26	2.38	V

		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.36	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.55	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.45	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.66	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.57	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.76	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.67	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.85	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.77	2.9	V
VPVDhyst(1)	PVD hysteresis	—	—	100	—	mV
VPOR/PDR	Power on/power down reset threshold	falling edge	—	1.90	—	V
		rising edge	—	2.02	—	V
VPDRhyst(1)	PDR hysteresis	—	—	30	—	mV
TRSTTEMPO(1)	Reset temporization	—	—	2	—	ms

(1) Guaranteed by design, not tested in production.

3.7 Embedded reference voltage

The parameters given in the table below are based on the VDD supply voltages listed under common operating conditions.

Table 14 Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VREFINT	Internal reference voltage	-40°C < TA < +85°C	1.16	1.20	1.24	V
TS_vrefint(1)	ADC sampling time when reading the internal reference voltage	—	—	5.1	17.1	us
TCoeff(2)	Temperature coefficient	—	—	—	100	ppm/°C

(1) Shortest sampling time can be determined in the application by multiple iterations.

(2) Guaranteed by design, not tested in production.

3.8 Supply current characteristics

The current consumption is a composite indicator of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code, etc.

The current consumption is measured as described in the Test Conditions chapter.

Current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned
- When the peripherals are enabled: fPCLK1 = fHCLK/2, fPCLK2 = fHCLK

Table 15 Current consumption in Run mode

Symbol	Parameter	Conditions	fHCLK	Typ(1)		Max(2)		Unit
				All peripherals enabled	All peripherals disabled	All peripherals enabled	All peripherals disabled	
IDD	Supply current in Run mode	External clock(3)	216MHz	36.29	25.49	38.50	27.56	mA
			168MHz	27.71	19.27	29.95	21.35	
			72MHz	13.09	9.38	14.93	11.21	
			48MHz	9.35	6.93	11.18	8.74	
			32MHz	6.88	5.25	8.68	7.04	
			24MHz	5.67	4.46	7.41	6.20	
			16MHz	4.43	3.63	6.16	5.34	
			8MHz	3.28	2.58	4.98	4.54	
		Runs on high-speed internal RC oscillator (HSI)	128MHz	21.64	15.19	23.89	17.27	mA
			72MHz	13.03	9.39	15.03	11.31	
			48MHz	9.34	6.92	11.26	8.78	
			32MHz	7.55	5.73	8.73	7.08	
			24MHz	5.69	4.49	7.74	6.24	
			16MHz	4.45	3.66	6.21	5.39	
			8MHz	3.30	3.88	5.02	4.57	

(1) The typical value is obtained by testing at TA=25℃, VDD=3.3V.

(2) The maximum value is obtained by testing at TA=85℃, VDD=3.6V.

(3) The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Power consumption of Ethernet

(Test Condition: VDD=3.3V, AVDD=3.3V, Ta = 25°C)

Table 16 Power Dissipation of Ethernet

Condition	Min	Typ	Max	Unit
100M Link	-	128	-	mA
10M Link	-	75	-	mA
Un-Link (Auto-negotiation mode)	-	65	-	mA
100M Transmitting	-	132	-	mA
10M Transmitting	-	79	-	mA
Power Down mode	-	13	-	mA

Current consumption in Sleep mode, code running from flash.

Table 17 Current consumption in sleep mode, where the code runs in Flash

(1) The typical value is obtained by testing at TA=25℃, VDD=3.3V.

Symbol	Parameter	Conditions	fHCLK	Typ(1)		Max(2)		Unit
				All peripherals enabled	All peripherals disabled	All peripherals enabled	All peripherals disabled	
IDD	Supply current in Sleep mode	External clock(3)	216MHz	25.72	7.01	27.73	8.70	mA
			168MHz	19.46	4.81	21.49	6.58	
			72MHz	9.53	3.25	11.31	4.92	
			48MHz	6.99	2.81	8.76	4.51	
			32MHz	5.32	2.54	7.07	4.23	
			24MHz	4.50	2.41	6.22	4.09	
			16MHz	3.66	2.28	5.36	3.96	
			8MHz	2.90	2.17	4.57	3.84	
		Runs on high-speed internal RC oscillator (HSI)	128MHz	15.31	4.14	17.36	5.90	mA
			72MHz	9.47	3.20	11.36	4.93	
			48MHz	6.97	2.80	8.80	4.52	
			32MHz	5.32	2.54	7.11	4.26	
			24MHz	4.49	2.41	6.25	4.12	
			16MHz	3.65	2.27	5.39	3.98	
			8MHz	2.89	2.17	4.61	3.87	

(1) The typical value is obtained by testing at TA=25℃, VDD=VBAT=3.3V.

(2) The maximum value is obtained by testing at TA=85℃, VDD=3.6V.

(3) The external clock is 8MHz, and the PLL is enabled when fHCLK>8MHz.

Table 18 Typical and maximum current consumption in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)	Max(2)	Unit
IDD	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and external high-speed oscillator OFF (no independent watchdog)	210	1290	uA
		Regulator in Low-power mode, low-speed and high-speed internal RC oscillators and external high-speed oscillator OFF (no independent watchdog)	150	1220	
	Supply current in Standby mode	Low-speed internal RC oscillator, external low-speed oscillator and RTC, IWDG OFF	0.7	2.2	
		Low-speed internal RC oscillator ON, external low-speed oscillator and RTC, IWDG OFF	1.0	2.5	
		External low-speed oscillator ON, low-speed internal RC oscillator and RTC, IWDG OFF	1.0	2.6	
		External low-speed oscillator and RTC ON, low-speed internal RC oscillator and IWDG OFF	1.3	2.7	
		Low-speed internal RC oscillator and IWDG ON, external low-speed oscillator and RTC OFF	1.0	2.7	
IDD_VBAT	Supply current in backup area	External low-speed oscillator and RTC ON	0.9	1.3	

(1) The typical value is obtained by testing at TA=25℃, VDD=VBAT=3.3V.

(2) The maximum value is obtained by testing at TA=85℃, VDD=VBAT=3.6V.

(3) Derived from comprehensive evaluation, not tested in production.

3.9 External clock source characteristics

High-speed external user clock generated from an external oscillator source

The characteristics given in the table below are measured using a high-speed external clock source, and the ambient temperature and supply voltage meet common operating conditions.

Table 19 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSE_ext	User external clock source frequency	—	0.615	8	35	MHz

VHSEH	OSC_IN input pin high level voltage		0.48Vdd	—	Vdd	V
VHSEL	OSC_IN input pin low level voltage		Vss	—	0.38Vdd	
tw(HSE)	OSC_IN high or low time		5	62.5	—	ns
tr(HSE) tf(HSE)	OSC_IN rise or fall time		—	4.1	20	
Cin(HSE)	OSC_IN input capacitance	—	—	5	—	pF
DuCy(HSE)	Duty cycle	—	45	50	55	%

Low-speed external user clock generated from external oscillator source

Table 20 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSE_ext	User external clock source frequency	—	—	32.768	1000	KHz
VLSEH	OSC32_IN input pin high level voltage		0.48Vdd	—	VDD	V
VLSEL	OSC32_IN input pin low level voltage		VSS	—	0.38Vdd	
tw(LSE) tw(LSE)	OSC32_IN high or low time		450	—	—	ns
tr(LSE) tf(LSE)	OSC32_IN rise or fall time		—	—	50	
Cin(LSE)	OSC32_IN input capacitance	—	—	5	—	pF
DuCy(LSE)	Duty cycle	—	30	—	70	%

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external clock (HSE) can be generated using an oscillator consisting of a crystal/ceramic resonator of 4~16MHz. The information given in this section is based on a comprehensive characterization using the typical external components listed in the table below.In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics(frequency, package, accuracy).

Note: The crystal resonator mentioned here is what we usually call passive crystal oscillator.

Table 21 HSE 4~16MHz oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fOSC_IN	Oscillator frequency	—	4	8	16	MHz

tSU(HSE)	Startup time	VDD is stabilized	TA = -40℃	—	790	—	us
			TA = 25 ℃	—	860	—	
			TA = 85 ℃	—	960	—	

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Note: The crystal resonator mentioned here is what we usually call passive crystal oscillator.

Table 22 LSE oscillator characteristics (fLSE=32.768kHz)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
tSU(HSE)(1)	Startup time	VDD is stabilized	TA = -40℃	—	321	—	ms
			TA = 25 ℃	—	221	—	
			TA = 85 ℃	—	223	—	

3.10 Internal clock source characteristics

The characteristic parameters given in the table below are measured using ambient temperature and supply voltage in accordance with common operating conditions.

High-speed internal (HSI) RC oscillator

Table 23 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fHSI	frequency	—	—	8	—	MHz
ACCHSI	Accuracy of the HSI oscillator	TA = -40~85℃	-2.5	—	2.5	%
tSU(HSI)	HSI oscillator startup time	—	—	12	—	us
IDD(HSI)	HSI oscillator power consumption	—	—	3.5	—	uA

Low-speed internal (LSI) RC oscillator

Table 24 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit

fLSI	frequency	–	38	40	42	kHz
tSU(LSI)	LSI oscillator startup time	–	–	75	–	us
IDD(LSI)	LSI oscillator power consumption	–	–	0.28	–	uA

3.11 Crystal Characteristics of Ethernet

Table 25 Crystalline properties of Ethernet

Parameter	Range
Frequency	25 MHz
Frequency Tolerance (at 25℃)	±30 ppm
Shunt Capacitance	7pF Max
Drive Level	59.12uW/MHz
Load Capacitance	18pF
Aging (at 25℃)	±3ppm / year Max

3.12 Wakeup time from low-power mode

The wakeup times is measured on a wakeup phase with a 8MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering sleep mode

All timings are derived from tests performed under ambient temperature

Table 26 Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
tWUSLEEP	Wakeup from sleep mode	10	CPU clock cycle
tWUSTOP	Wakeup from stop mode(regulator in low-power mode)	12	us
tWUSTDBY	Wakeup from standby mode	1600	us

3.13 PLL characteristics

The parameters listed in the table below are measured using ambient temperature and supply voltage in accordance with common operating conditions.

Table 27 PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
fPLL_IN	PLL input clock(2)	1	8	32	MHz
	PLL input clock duty cycle	40	–	60	%

fPLL_OUT	PLL multiplier output clock	4	—	216	MHz
tLOCK	PLL lock time	—	51.2	87.8	us
Jitter	Cycle-to-cycle jitter	—	—	200	ps

(1) Derived from a comprehensive evaluation, not tested in production.

(2) Care needs to be taken to use the correct frequency multiplier so that the fPLL_OUT is within the allowable range based on the PLL input clock frequency.

3.14 Memory characteristics

Flash memory

The characteristics are given at TA = –40 to 85 °C unless otherwise specified.

Table 28 Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Unit
tPROG	16-bit programming time	—	50	us
tERASE	Page erase time	—	25	ms
tME	Mass erase time	—	6	s

Table 29 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
NEND	Endurance	TA = -40~85℃	100	—	—	kcycles
tRET	Data retention	TA = 105℃	20	—	—	years

3.15 Absolute maximum ratings (electrical sensitivity)

Electrostatic discharge(ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test is compliance with the JESD22-A114/C101 standard.

Table 30 ESD absolute maximum ratings

Symbol	Parameter	Conditions	Type	Max	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA =+25 °C, confirming to JEDEC EIA/JESD22-A114	3A	4000	V

3.16 I/O port characteristics

General input/output characteristics

Table 31 I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low level input voltage	–		–	1.38	V
VIH	Standard IO input high level voltage		1.59	–	–	
	IO FT input high level voltage		1.59	–	–	
Vhys	Standard IO Schmitt trigger voltage hysteresis	–	–	0.21	–	V
	5V tolerance IO Schmitt trigger voltage hysteresis		–	0.21	–	V
Ilkg	Input leakage current	VSS ≤ VIN ≤ VDD Standard I/Os	–	–	±0.5	uA
		VIN = 5V, 5V tolerance port	–	–	±1	
RPU	Weak pull-up equivalent resistor	VIN = VSS	37	–	38.5	kΩ
RPD	Weak pull-down equivalent resistor	VIN = VDD	43.7	–	45.7	kΩ
CIO	I/O pin capacitance			5		pF

Output voltage

Table 32 Output Voltage Characteristics

Symbol	Parameter	Conditions	Min	Max	Max
VOL	Output low level voltage	TTL port, I_{IO} = +12mA		0.4	V
VOH	Output high level voltage	VDD=3.3V	2.9		
VOL	Output low level voltage	CMOS port, I_{IO} = +14mA		0.4	
VOH	Output high level voltage	VDD=3.3V	2.9		
VOL	Output low level voltage	I_{IO} = +34mA		1.3	
VOH	Output high level voltage	VDD=3.3V	2		

3.17 NRST pin characteristics

Table 33 NRST pin characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit

VIL(NRST)	NRST Input low level voltage	–	–	1.31	–	V
VIH(NRST)	NRST Input high level voltage	–	–	1.57	–	
Vhys(NRST)	NRST Schmitt trigger voltage hysteresis	–	–	260	–	mV
RPU	Weak pull-up equivalent resistor	VIN=VSS	–	37	–	kΩ
VF(NRST)	NRST Input filtered pulse	–	–	120	–	ns
VNF(NRST)	NRST Input not filtered pulse	–	25	–	–	ns

3.18 TIM timer characteristics

Table 34 TIMx characteristics

Symbol	Parameter	Min	Max	Unit
tres(TIM)	Timer resolution time	1	–	tTIMxCLK
fEXT	Timer external clock frequency on CH1 to CH4	0	FTIMCLK/2	MHz
ResTIM	Timer resolution	–	16	bit
tCOUNTER	16-bit counter clock period when internal clock is selected	1	65535	tTIMxCLK
tMAX_COUNT	Maximum possible count	–	65535*65535	tTIMxCLK

3.19 CAN (controller area network) interface

For more information on the characteristics of the input/output multiplexing function pins (CAN_TX and CAN_RX), see the IO Port Characteristics section.

3.20 12-bit ADC characteristics

Table 35 ADC characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VDDA	Power supply	–	2.0	3.3	3.6	V
VREF+	Positive reference voltage	–	2.0	–	VDDA	V
fADC	ADC clock frequency	–	0.6	–	14	MHz
fS	Sampling rate	–	0.05	–	1	MHz
fTRIG	External trigger frequency	fADC = 14MHz	–	–	823	kHz
VAIN	Conversion voltage range	–	0		VREF+	V

RAIN	External input impedance	–	–	–	50	kΩ
RADC	Sampling switch resistance	–	–	–	1	kΩ
CADC	Internal sample and hold capacitor	–	–	–		pF
tCAL	Calibration time	fADC = 14MHz	5.9			us
			83			1/fADC
tlat	Injection trigger conversion latency	fADC = 14MHz	–	–	0.214	us
			–	–	3	1/fADC
tlatr	Regular trigger conversion latency	fADC = 14MHz	–	–	0.143	us
			–	–	2	1/fADC
tS	Sampling time	fADC = 14MHz	0.107	–	17.1	us
			1.5	–	239.5	1/fADC
tSTAB	Power-up time	–	0	0	1	us
tCONV	Total conversion time (including sampling time)	fADC = 14MHz			18	us
			14 to 252 (tS for sampling +12.5 for successive approximation)			1/fADC

Table 36 RAIN max for fADC = 14MHz

TS(cycles)	tS(us)	Max RAIN(kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	-
239.5	17.11	-

3.21 DAC electrical parameters

Table 37 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Remark
VDDA	Analog supply voltage	2.0	-	3.6V	V	
VREF+	Reference voltage	2.0	-	3.6V	V	VREF+ must always be lower than VDDA
VSSA	Ground wire	0	-	0	V	-
RLOAD	Load resistance with buffer open	5	-	-	kΩ	-
RO	Output impedance with buffer off	-	-	15	kΩ	-
CLOAD	Load capacitance	-	-	50	pF	Bulk capacitor on DAC_OUT pin (buffer on)
DAC_OUTsmall	DAC_OUT voltage on low side when buffer is on	50	-	-	mV	Gives the maximum DAC output span
DAC_OUTbig	DAC_OUT voltage on high side when buffer is on	-	-	VREF+ - 0.2	V	
DAC_OUTsmall	DAC_OUT voltage on low side with buffer off	-	0.5	-	mV	Gives the maximum DAC output span
DAC_OUTbig	DAC_OUT voltage on high side with buffer off	-	-	VREF+ - 0.03	V	
DNL	Nonlinear distortion (deviation between 2 consecutive codes - 1LSB)	-	-	+-2	LSB	DAC configured as 12-bit
INL	Nonlinear accumulation (deviation between the value measured at code i and the line between code DAC_OUT large and code DAC_OUT small)	-	-	+-4	LSB	DAC configured as 12-bit
Offset Error	Offset error (the deviation between the measured value at code 0x800 and the ideal value V REF+ /2)	-	15	25	mV	With VREF+ = 3.3 V, the DAC is configured as 12-bit
tSETTLING	Setup time (full scale: 10-bit input code transitions from small to large, DAC_OUT reaches ±1 LSB of its final value)	-	3	4	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ

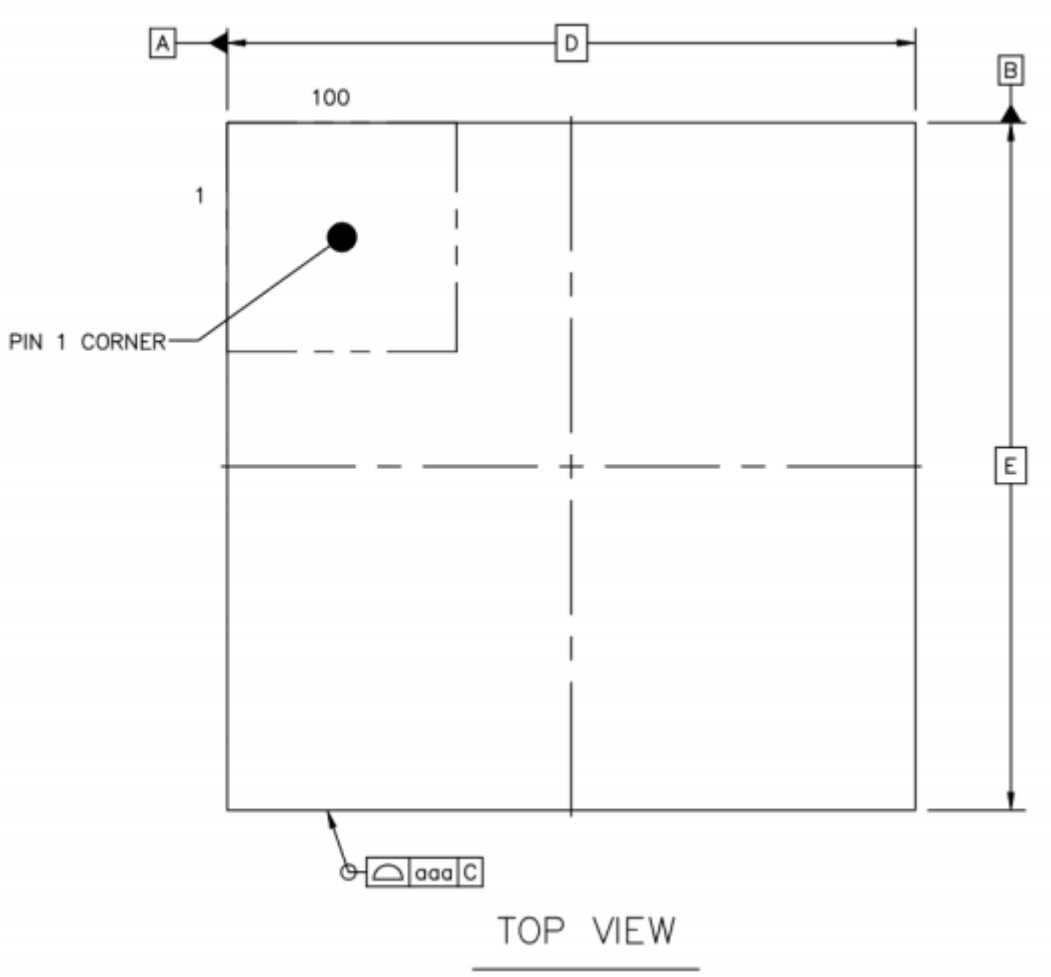
Update rate	When the input code is a small change (from the value i to i+1 LSB), the large frequency of the correct DAC_OUT is obtained	-	-	1	MS/s	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ
tWAKEUP	Time to wake up from off state (set ENx bit in DAC control register)	-	6.5	10	us	C LOAD ≤ 50 pF, R LOAD ≥ 5kΩ input code between small and large possible values
PSRR+	Supply rejection ratio (relative to VDDA) (static DC measurement)	-	-60	-50	dB	Without R LOAD , C LOAD ≤ 50 pF

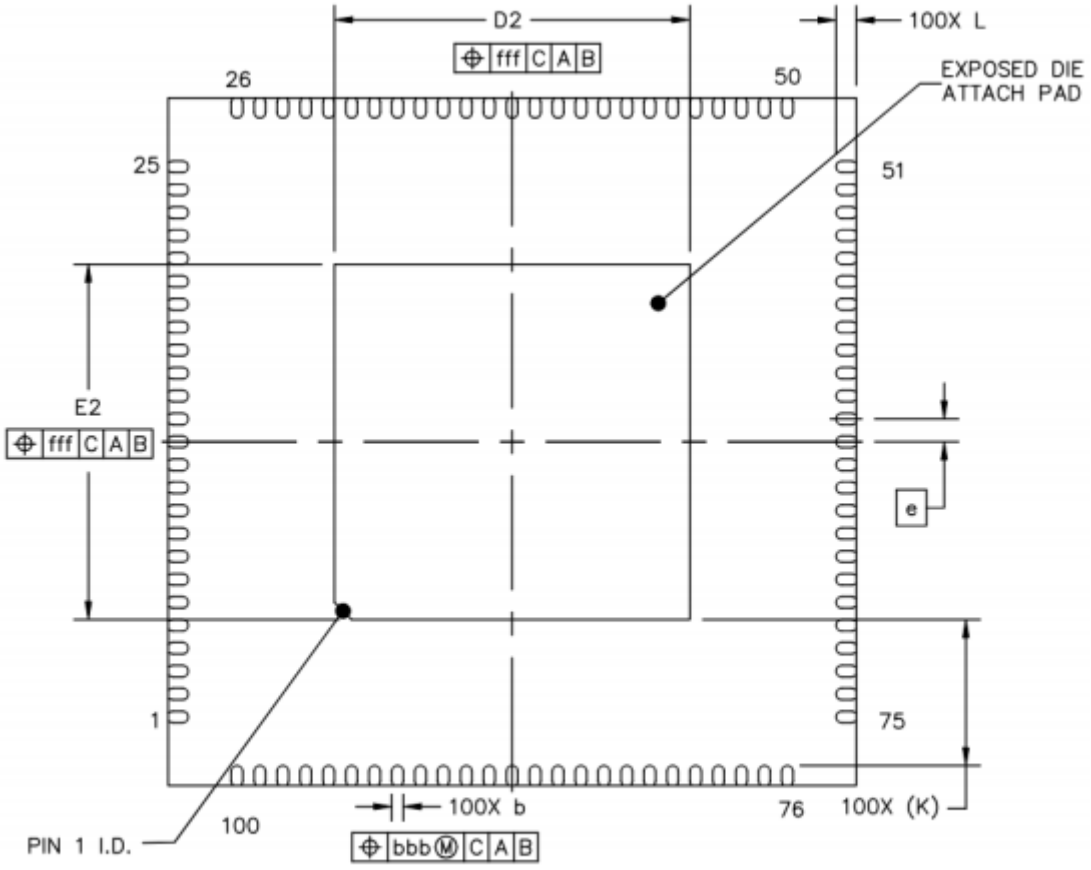
3.22 Temperature sensor characteristics

Table 38 Temperature sensor characteristics

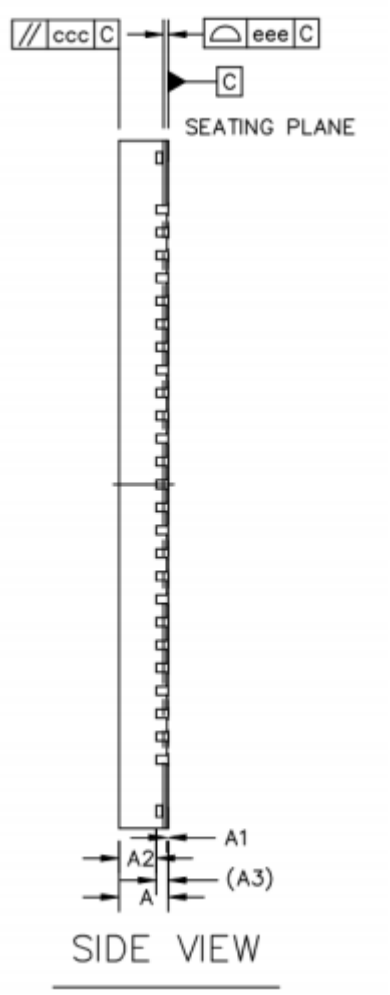
Symbol	Parameter	Min	Typ	Max	Unit
Avg_Slope	Average slope	—	5	—	mV/°C
V25	Voltage at 25 °C	—	1.43	—	V
tSTART	Startup time	—	—	10	us
TS_temp	ADC sampling time when reading the temperature	—	—	17.1	us

4 Package Information



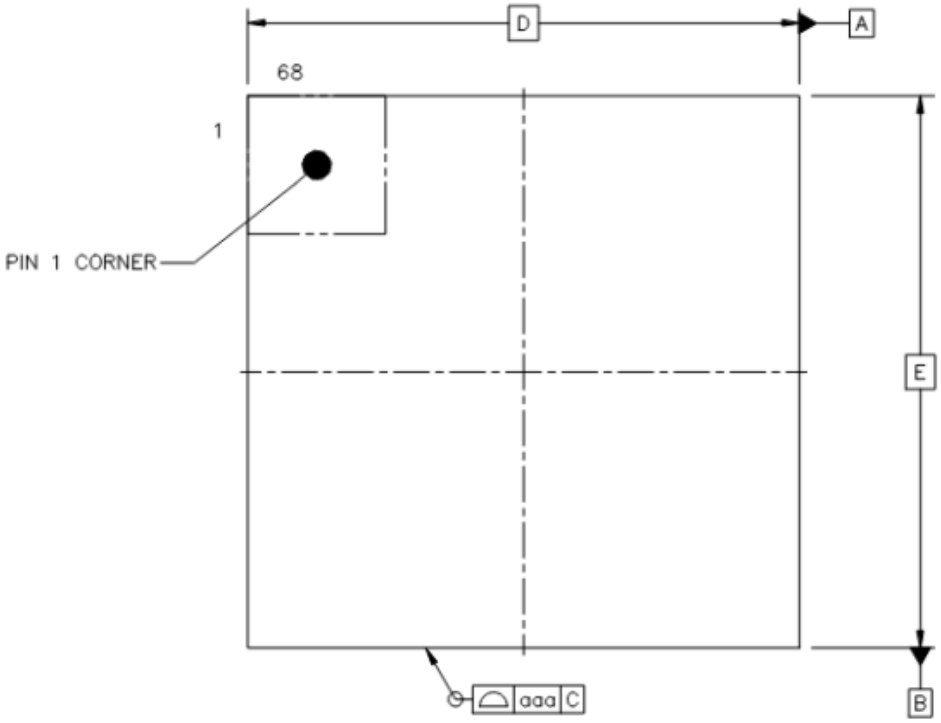

D2
fff C A B
100X L
EXPOSED DIE
ATTACH PAD
26
50
25
51
E2
fff C A B
e
1
75
100X b
bbb M C A B
100
76
100X (K)
PIN 1 I.D.

BOTTOM VIEW

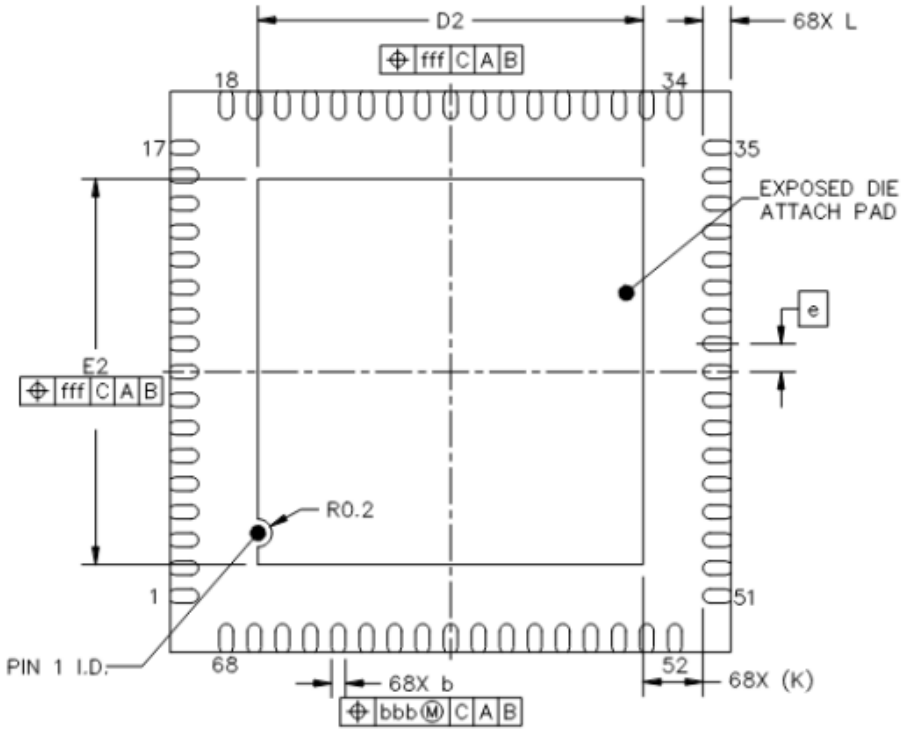


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	1.05	1.1	1.15
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.9	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		12 BSC	
	Y	E		12 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	6.1	6.2	6.3
	Y	E2	6.1	6.2	6.3
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		2.55 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

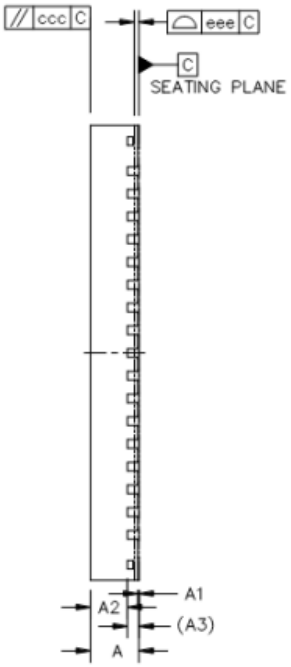
Figure 3 W55MH32L pack



TOP VIEW



BOTTOM VIEW



SIDE VIEW

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	5.4	5.5	5.6
	Y	E2	5.4	5.5	5.6
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.85 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

Figure 4 W55MH32Q pack

5 Document History Information

Version	Date	Descriptions
Ver. 1.0.0	2024-10-31	Initial Release

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Sales & Distribution: sales@wiznet.hk
For more information, visit our website at http://www.wiznet.io