

Identification No.: UJGBYB



QRT Inc.

Reliability Test Report

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COMPANY : WIZnet Co., Ltd

PRODUCT : W5500

PACKAGE : 48 LQFP

PURPOSE : Qualification

ISSUED DATE : Aug 08, 2016

REFERENCE No. : IRRQ-1511-01132

Prepared by : Jaeyol Kim

Approved by : Changjoon Lee

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2091 Gyeongchung-daero Bubal-eub Icheon-si Gyeonggi-do, Korea Tel. 82-31-8094-8231 Fax. 82-31-8094-8240 www.qrtkr.com



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1 Qualification Plan and Results

The purpose of these tests is evaluation (or monitoring) of W5500.

Test conditions are specified in customers in-house test plan and all test procedures comply with JEDEC standards.

Obligation to perform exact procedure to reference documents is QRT Inc. responsibility only, but establishing failure criteria and judgment of pass/fail is customer's responsibility.

TEST MODE	TEST CONDITION	TEST TIME	SAMPLE SIZE	FAILED UNIT ¹⁾	REF. DOCUMENT ²⁾
High Temperature Operating Life	125 °C ± 5 °C V0 = 3.3 V, V1 = 3.3 V VIH = 3.3 V	504 h	77	0	JESD22-A108D : 2010
Low Temperature Operating Life	-40 °C ± 5 °C V0 = 3.3 V, V1 = 3.3 V VIH = 3.3 V	504 h	77	0	JESD22-A108D : 2010

Additional Requirement: N/A

NOTE

1) Test results are based on the "Final Test Result" provided by Customer.

2) Although the name of test item is same, reference documents can be JEDEC, MIL-std or AEC.



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2 Test Vehicles

Manufacturer: WIZnet Co., Ltd

Part Number: W5500

Description: -

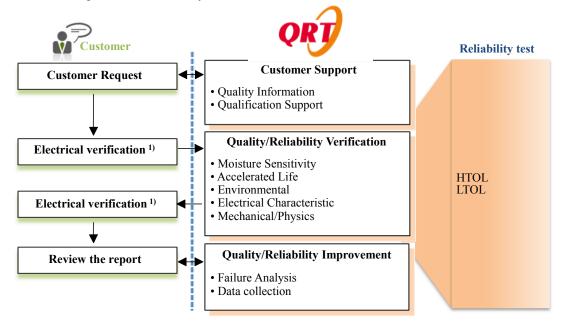
Package Type: 48 LQFP

Ass'y Site: -

Fab Site: -

3 Test Flow/Procedure

All reliability tests performed by QRT Inc. comply with international standard. QRT Inc. provide customer support featuring easy-understanding documents & technical information. And product monitoring activities to confirm quality and reliability level by sampling inspection and reliability test.



NOTE 1) Customer's Responsibilities only. Electrical Test can be omitted depending on customer's request

Figure 3-1. Reliability Test Flow



4 Reliability Tests

4.1 High Temperature Operating Life (HTOL)

The High Temperature Operating Life (HTOL) or steady-state life test is performed to determine the reliability of devices under operation at high temperature conditions over an extended period of time. It consists of subjecting the parts to a specified bias or electrical stressing, for a specified amount of time, and at a specified high temperature.

Conditions			
User Temp (Tu)	55	Test Temp (Tt)	125 °C ± 5 °C
User Voltage (Vu)	0	Test Voltage (Vt)	VDD = MAX
Activation Energy (Eaa)	0.7	$\gamma V = (K/X)$	5.5
Sample size (N)	77	failures (f)	
Test duration (t _A)	504 h	t _{life} (for ppm)	12

Life estimate is calculated on the assumption that 1) Gate short to source or drain *, 2) User temp is 55 °C.

------Calculation-----

Acceleration Factor (AF) = $\exp\{(E_{aa}/k)(1/Tuse - 1/Ttest)\}$

where

 E_{aa} = apparent activation energy in eV/atom

 $k = Boltzmann's constant (8.62 \times 10^{-5} eV/K)$

 T_{use} = use temperature in kelvins

 T_{test} = Test temperature in kelvins

$$= \exp[(0.7/k) \times (1/328 - 1/398)] = 77.94$$

$$\therefore$$
 Test time = AF × Test Time = $77.94 \times 504 \text{ h} = 4.48 \text{ years}$

if Exponential distribution (FIT Calculation)

The degrees of freedom = 2, and χ^2 = 1.83 @ CL 60%

Failure rate (in FIT) = $10^9 \times \chi^2_{c,d} / (2 \times AF \times N \times t_A)$

$$= 10^9 \times 1.83 / (2 \times 77.94 \times 77 \times 504 \text{ h}) = 302.51 \text{ FIT}$$

- : Failure Rate (in ppm, 12 months) = 2650 ppm during the first 12 months of usage.
- \therefore MTTF = 377 years

! Disclaimer !

This estimation is an example of JESD74A. Voltage Acceleration is excluded in this procedure. Voltage acceleration and actual use temperature must be considered for a better output. Calculation is for information only.

^{*}Failure Mode: Gate short to source or drain

^{*}Failure Mechanism: Intrinsic breakdown; for gate oxide thickness >4 nm

^{*} $E_{aa} = 0.7$ (activation energy reference "JEP122D")



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4.2 Low Temperature Operating Life (LTOL)

This test is performed to determine the reliability of devices under operation at high temperature conditions over an extended period of time. It is intended to look for failures caused by hot carriers, and is typically applied on memory devices or devices with submicron device dimensions.

Test condition

Chamber condition : -40 $^{\circ}$ C ± 5 $^{\circ}$ C Bias configuration : VDD=MAX

Duration : 504 h Sample Size : 77 ea



APPENDIX A: HTOL Test Conditions

1. Bias Configuration

Test Item: High Temperature Operating Life	Test condition : Room	
V0 : 3.3 V V1 : 3.3 V	VIH: 3.3 V VIL: 0 V	
Vector Type : pattern.dat	Cycle Time: 1000 ns	
Timing Format Condition		
* XI : 1Mhz		

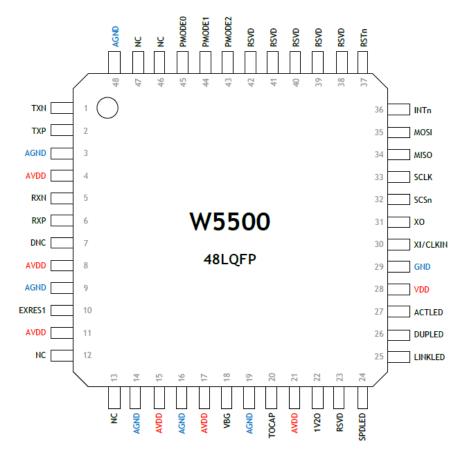
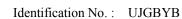


Figure 1. W5500 Pin Layout





2. HTOL Socket Board



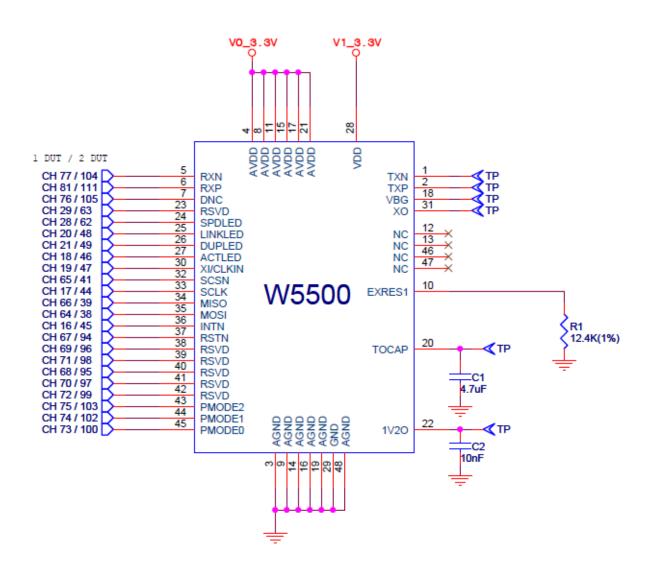
Figure 2-1 HTOL Socket Board

2.1 Information

Model / Device	48LQFP / W5500	Socket SPEC	55-023-167-01
Customer	WIZnet Co., Ltd	Socket Vendor	ENPLAS
Pitch / Type / Body Size	0.5P / LQFP / 7X7	BOARD S/N	AQR15281A
QTY	40 ea	Vendor	AD&T
BOARD TYPE	HTOL SOCKET BOARD	Receive Date	2015.11.11

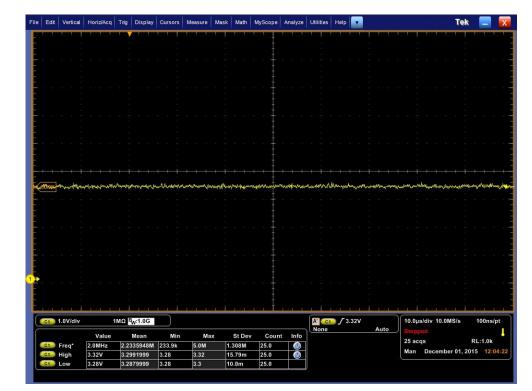


3. HTOL Board Circuit





4. Power Waveform



V0:3.3V



V1:3.3V



5. Output Waveform



VBG (18)



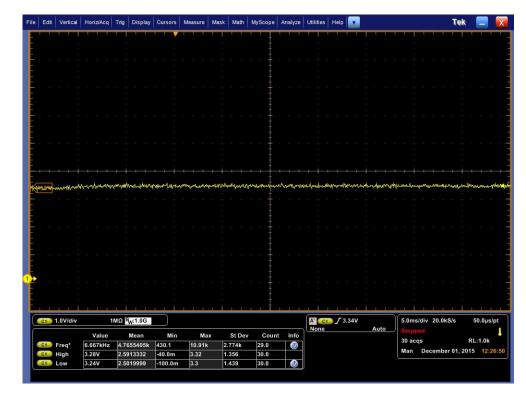
TOCAP (20)



5. Output Waveform



1V2O (22)

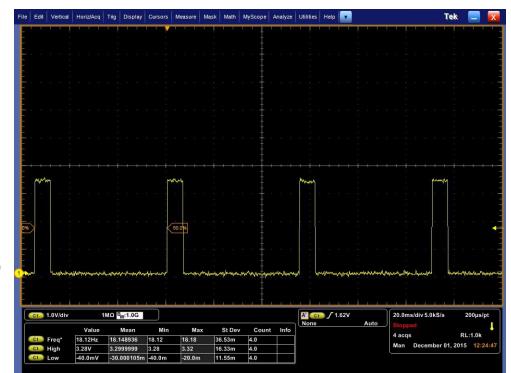


LINKLED DUPLED ACTLED





5. Output Waveform



SPDLED (24)



5. Output Waveform











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Icheon Head Office	2091, Gyeongchung-daero, Bubal-eub, Icheon-si, Gyeonggi-do, KOREA 467-701
	Tel. 82-31-8094-8231 Fax 82-31-8094-8240
Cheongju Branch	215, Daesin-ro, heungdeok-gu, Cheongju-si, Chungcheongbuk-do, KOREA 361-725
	Tel. 82-43-280-3955 Fax 82-43-280-2653
Gumi Branch	31-22, 1gongdan-ro 10-gil, Gumi-si, Gyeongsangbuk-do, KOREA, 730-723
	Tel. 82-54-470-1528, Fax 82-54-472-8031

Contact Information (Icheon) Tel. 82-31-8094-8231 Changjoon.lee@qrtkr.com